IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., Plaintiff, v. FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION, Defendants.	)	**REDACTED PUBLIC VERSION** C.A. No. 04-1371-JJF

COMBINED APPENDIX TO DEFENDANTS': (i) OPENING POST-TRIAL BRIEF IN SUPPORT OF THEIR ASSERTION THAT THE PATENTS-IN-SUIT ARE UNENFORCEABLE DUE TO INEQUITABLE CONDUCT; AND (ii) PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW REGARDING THE UNENFORCEABILITY OF THE PATENTS-IN-SUIT DUE TO INEQUITABLE CONDUCT

(VOLUME IV of V)

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United States Patent [19]

Balakrishnan et al.

[11] Patent Number: 5,245,526

[45] Date of Patent: Sep. 14, 1993

[54] BELOW GROUND CURRENT SENSING WITH CURRENT INPUT TO CONTROL THRESHOLD

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[73] Assignee: Power Integrations, Inc., Mountain View, Calif.

[21] Appl. No.: 832,227

[22] Filed: Feb. 7, 1992

[51] Int. Cl.[5] H02M 3/335

[52] U.S. Cl. 363/97; 307/362; 323/284

[58] Field of Search 363/21, 97, 131; 323/282, 284; 361/93; 307/362

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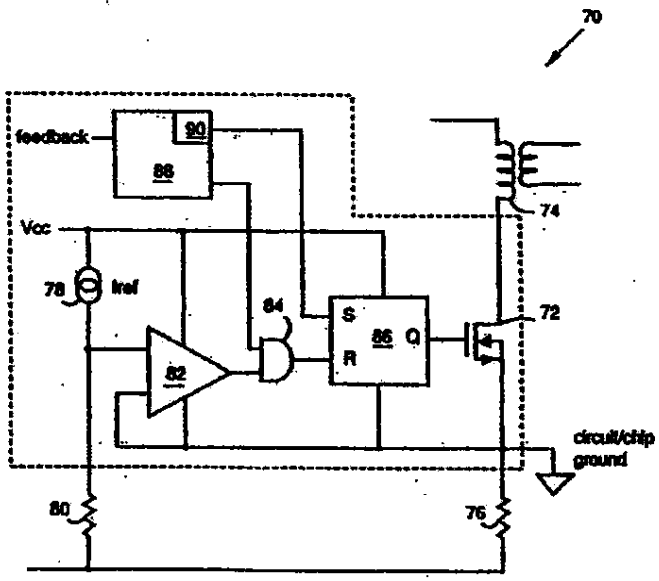
Primary Examiner—William H. Beha, Jr.
Attorney, Agent, or Firm—Thomas E. Schatzel

[57] ABSTRACT

An embodiment of the present invention is a switching power supply with high voltage positive and negative power inputs, a system ground, a sensing resistor placed between the negative power input and system ground, first and second load outputs with the first load output connected to the positive power input, and a comparator having first and second comparison inputs and a comparison output with the second comparison input connected to the system ground. A constant-current source is connected to the first comparison input of the comparator. A power MOSFET switch transistor has its drain connected to the second load output, its source connected to the system ground, and its gate controlled by the comparison output of the comparator. And a control resistor is connected between the second power input and said first comparison input of the comparator. The constant-current source, control resistor, and sensing resistor are such that when a predetermined current flowing through the first and second load outputs reaches a predetermined level (the current limit), the voltage developed across the sensing resistor will be equal to the voltage dropped across the control resistor, and the comparator will turn off the transistor to prevent further current increases.

8 Claims, 6 Drawing Sheets



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DEFT Exhibit No. DX 1000
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Signature _____

Fig._1
(prior art)

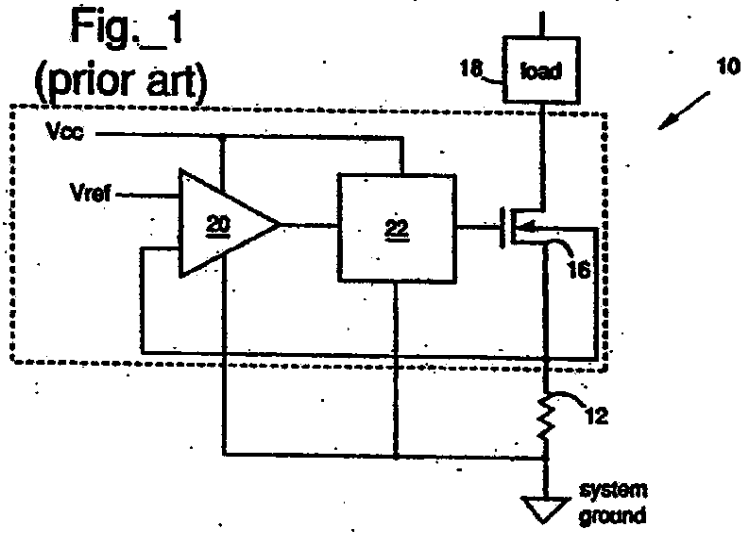


Fig._2
(prior art)

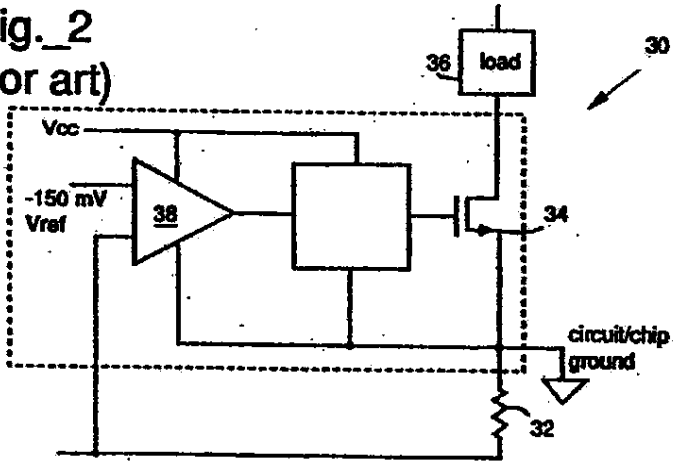
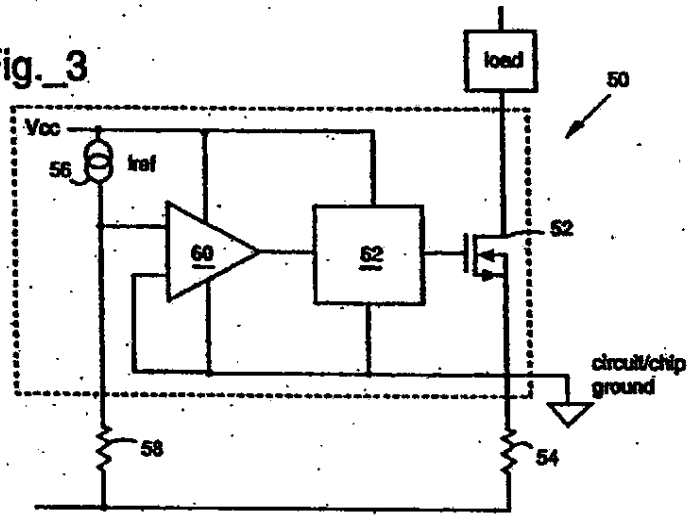


Fig._3


load
50
Vcc
56
Iref
60
62
52
circuit/chip ground
58
54

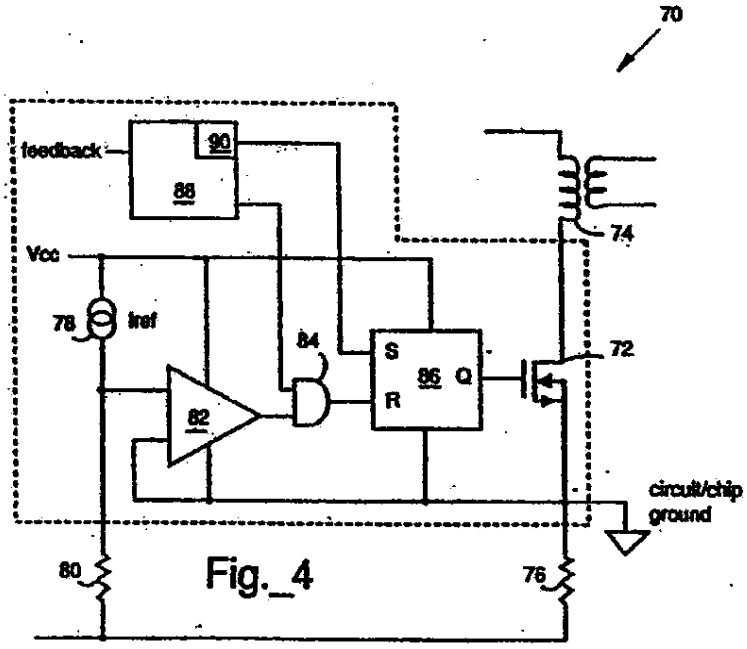
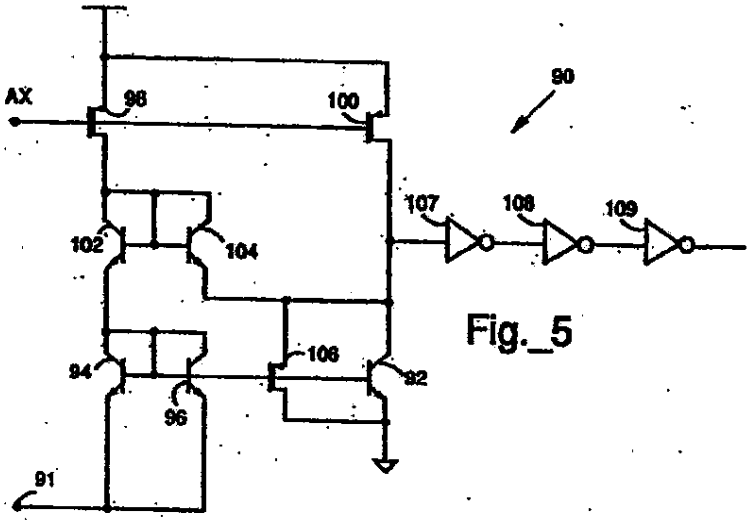

70
feedback
90
88
Vcc
74
78
Iref
84
S
86
Q
R
72
82
circuit/chip ground
80
76

Fig._4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90
107
108
109
102
104
106
94
92
96
91

Fig._5

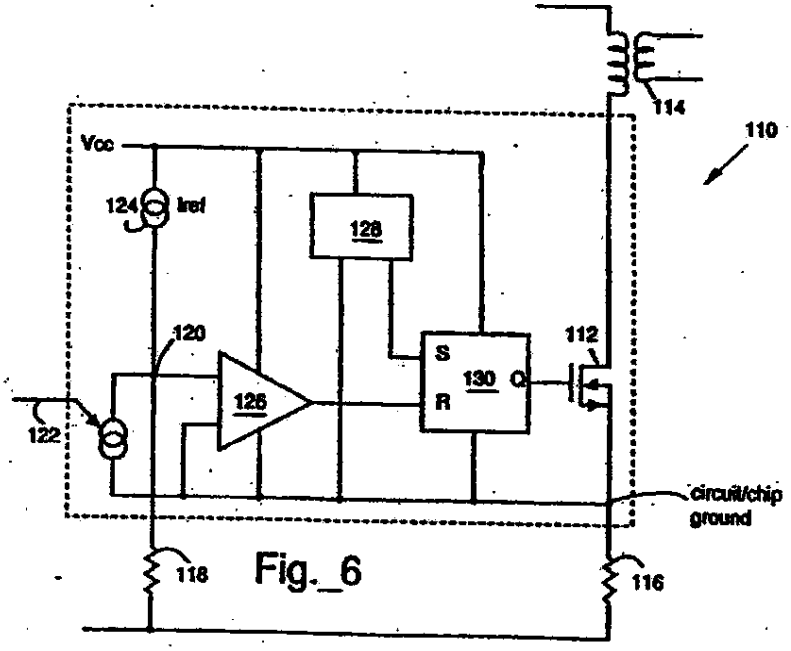
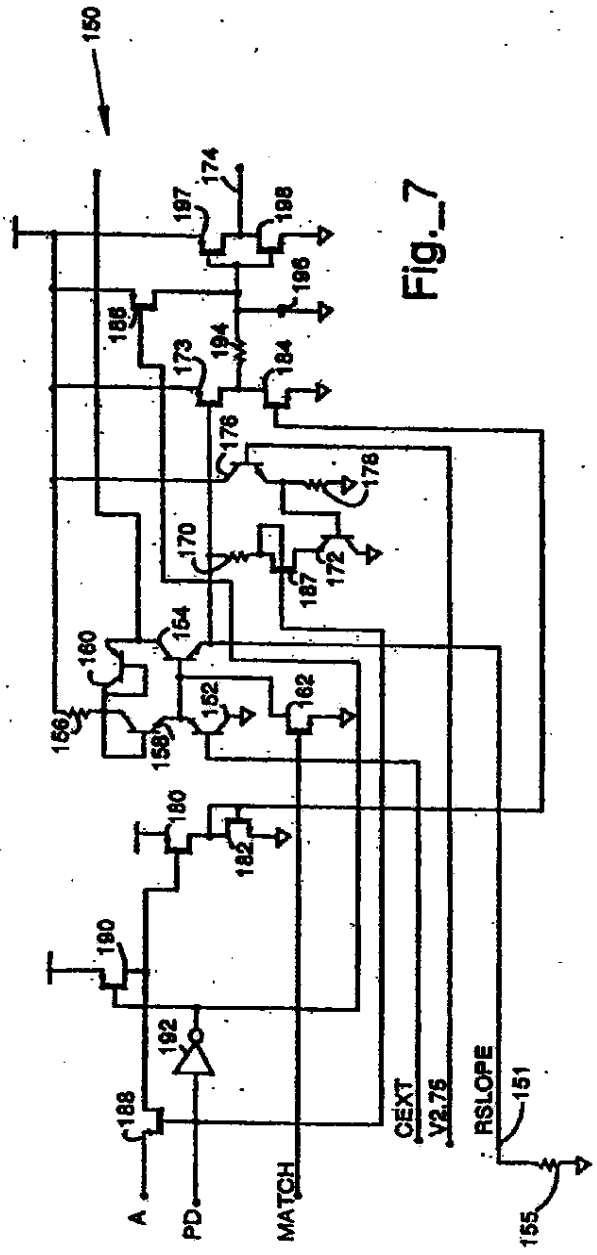

114
110
Vcc
124
Iref
128
120
112
S
130
Q
R
126
122
circuit/chip ground
118
116

Fig._6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174
197
198
196
185
173
194
184
176
178
170
172
187
164
160
162
156
158
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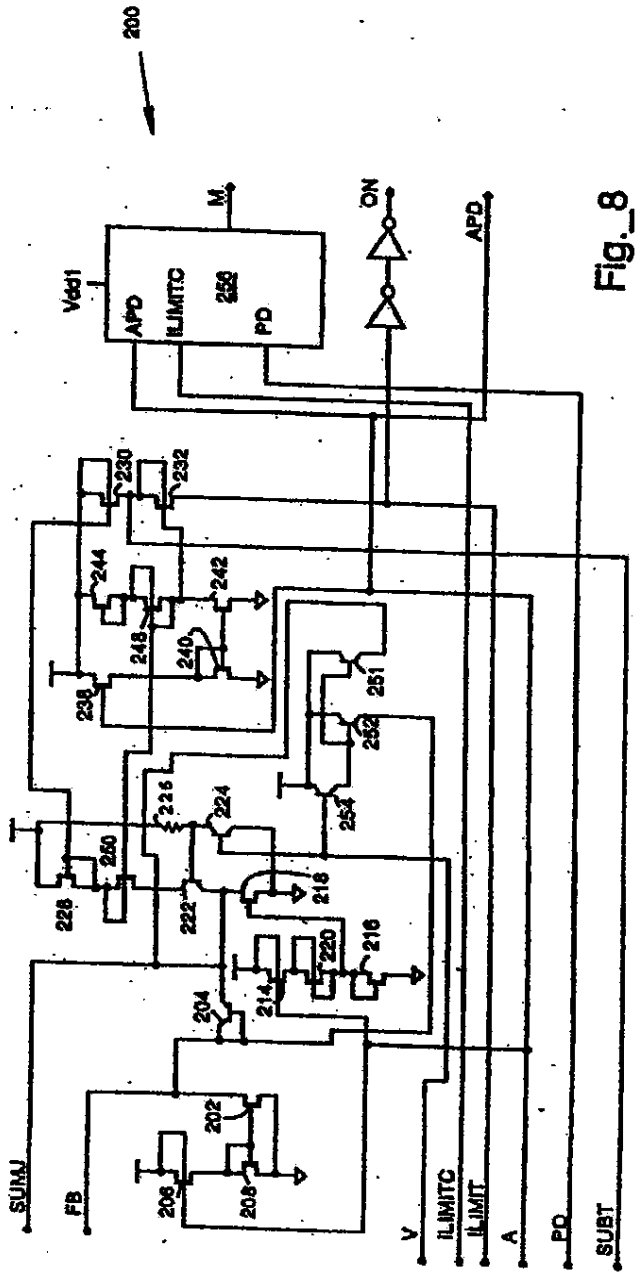
182
190
192
188
A
PD
MATCH
CEXT
V2.75
RSLOPE
151
155

Fig._7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M
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APD
Vdd
APD
ILIMITC
PD
230
232
244
242
248
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238
251
252
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226
224
250
218
228
222
220
216
214
204
202
206
208
SUM
FB
V
ILIMITC
ILIMIT
A
PD
SUBT

Fig. 8

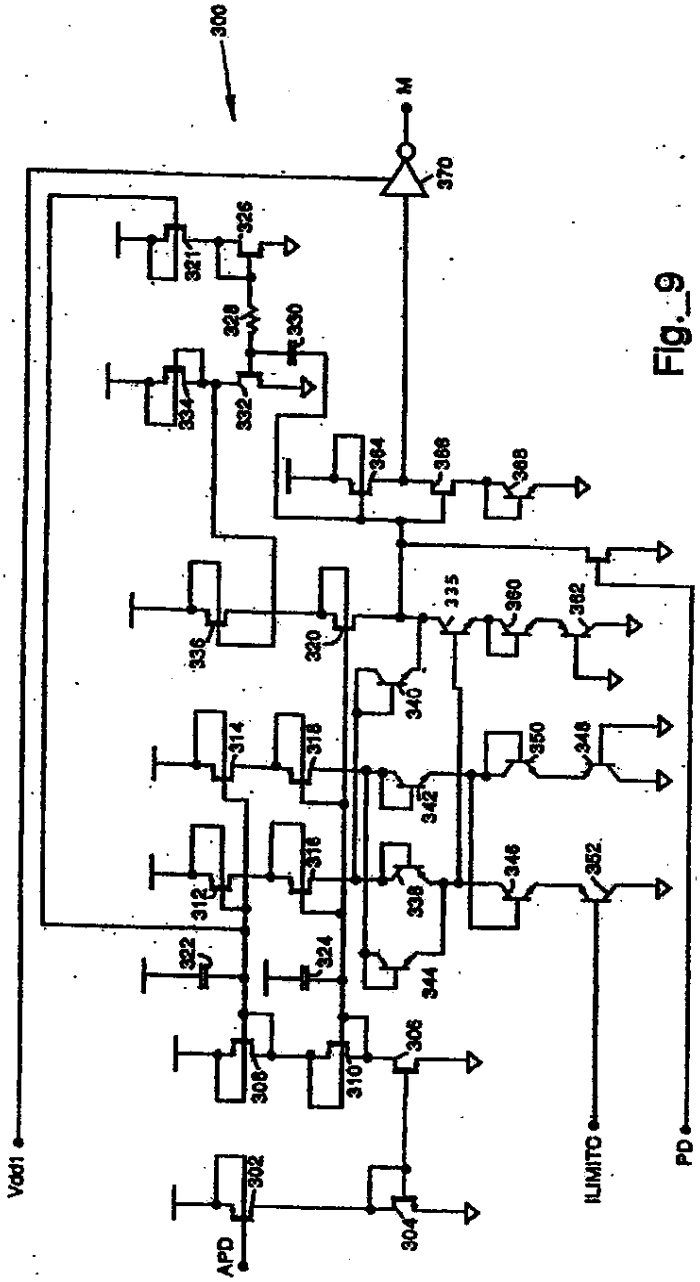
300
M
370
326
321
328
330
334
332
364
366
368
336
320
335
360
362
340
314
318
350
348
342
316
312
346
352
338
322
324
344
306
308
310
302
304
APD
Vdd1
ILIMITO
PD

Fig._9

BELOW GROUND CURRENT SENSING WITH CURRENT INPUT TO CONTROL THRESHOLD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to electronic power supplies and specifically to methods of measuring and limiting current delivered to a load.

2. Description of the Prior Art

Two types of power supplies are in wide use that convert an incoming source to voltage levels useful to the equipment being powered. Linear power supplies are the simplest, a series transistor typically, drops enough voltage across it to maintain a constant output voltage. The problem with linear power supplies is that the heavier the output load, the more current will have to pass through the regulating transistor, since it is in series with the load. This increased current means more power must be dissipated by the transistor, and this power is thrown away as heat. Switching power supplies are more efficient and run cooler than linear power supplies at the same power levels. But switching power supplies are more complicated because a transistor operated as a switch is used to chop incoming current for a transformer that has the load connected to its secondary winding, usually through a rectifier and filter. A feedback circuit is needed to monitor the output voltage and increase the time duration the chopping transistor is on when more output voltage is needed and to reduce the time duration when less output voltage is needed. The feedback circuit often makes use of a third winding of the transformer. The advantages of the switching power supply are that they can operate either as step-up or step-down supplies, by adjusting the number of series conductors in the primary and secondary windings of the transformer, and less heat is dissipated by the transistor since it never operates in its linear region. The transistor is either fully off or fully on.

A problem develops in power supplies that use current limiting. A conventional method of current limiting for a pulse width modulation (PWM) type switching power supply is shown in FIG. 1. A power supply 10 has a resistor (Rs) 12 in series with a power switch transistor 16 and a load 18. A sense voltage (Vs) develops across Rs 12 that is the product of the current and the resistance (Ohm's Law). This voltage is sensed by an input of an comparator 20 and compared to a reference voltage (Vref). A logic block 22 accepts the comparison from comparator 20 and controls the gate of transistor 16. As Vs exceeds Vref, transistor 16 will turn off. When Vs drops below Vref, transistor 16 will turn on. The total effect is to limit the current through transistor 16, and therefore load 18, to a value that can be adjusted by Vref. The disadvantages of putting Rs 12 where it is, include reduced gate drive at higher currents because the Vt of transistor 16 increases and the source lifts from ground as more Vs develops. To combat this, the value of Rs 12 is kept very low, on the order of 0.1 ohms. But at such low resistance values, the trace resistance on a printed circuit board can become significant, and can ruin any precision. An accurate reference source is needed to produce Vref. And low values of Vs, which can typically be 200 millivolts, do not compete with noise very well. The current mode control which requires dynamic adjustment of the current limit based on several control inputs is difficult to implement.

In FIG. 2, a switching power supply control circuit 30 puts a sense resistor (Rs) 32 "below ground." A current (Is) through Rs 32 also passes through a switch transistor 34 and a load 36. A negative sense voltage (−Vs) develops across Rs 32 as a result of Is because circuit or chip ground is at the junction of Rs 32 and transistor 34. An comparator 38 must have a negative reference voltage (−Vref) so that it can compare −Vs. Although the problem of transistor source terminal lifting has been avoided, the negative −Vref is troublesome to derive. Only small threshold voltages can be used (e.g., 150-200 millivolts) if power supply 30 is implemented mostly on a chip, larger thresholds will forward bias the substrate of the chip.

What is needed is a method and apparatus for accurate current limiting without the problems inherent in the prior art.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide a switching power supply with improved current limiting characteristics.

Briefly, an embodiment of the present invention is a switching power supply with high voltage positive and negative power inputs, a system ground, a sensing resistor placed between the negative power input and system ground, first and second load outputs with the first load output connected to the positive power input, and a comparator having first and second comparison inputs and a comparison output with the second comparison input connected to the system ground. A constant-current source is connected to the first comparison input of the comparator. A power MOSFET switch transistor has its drain connected to the second load output, its source connected to the system ground, and its gate controlled by the comparison output of the comparator. And a control resistor is connected between the second power input and said first comparison input of the comparator. The constant-current source, control resistor, and sensing resistor are such that when a predetermined current flowing through the first and second load outputs reaches a predetermined level (the current limit), the voltage developed across the sensing resistor will be equal to the voltage dropped across the control resistor, and the comparator will turn off the transistor to prevent further current increases.

An advantage of the present invention is that gate drive is constant and independent of output current.

Another advantage of the present invention is that larger sense resistor values can be used because Vs no longer subtracts away from output transistor gate drive.

Another advantage of the present invention is that no voltage reference is necessary.

Another advantage of the present invention is that the current limit can be easily programmed by the control resistor R_{CL}, which is a much larger value than is found in the prior art.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

IN THE DRAWINGS

FIG. 1 is a block diagram of a prior art switching power supply with a sense resistor between the switching transistor and ground;

FIG. 2 is a block diagram of a prior art switching power supply with below ground voltage sensing;

FIG. 3 is a block diagram of a switching power supply, according to an embodiment of the present invention;

FIG. 4 is a block diagram of a voltage mode PWM controller power supply, according to an embodiment of the present invention;

FIG. 5 is a schematic diagram of a comparator suitable for use in the power supply of FIGS. 3 and 4;

FIG. 6 is a block diagram of a current mode controller, according to an embodiment of the present invention; and

FIG. 7 is a schematic diagram of a slope compensator, as used in FIG. 6;

FIG. 8 is a schematic diagram of an exemplary summing junction, such as used in FIG. 7; and

FIG. 9 is a schematic diagram of an exemplary summing junction comparator, as used in FIG. 8.

DETAILED DESCRIPTION OF THE EMBODIMENTS

In FIG. 3, a first embodiment of the present invention is a switching power supply 50 comprising a switching transistor 52, a sense resistor (R_S) 54, a constant current source 56, a current limit resistor (R_{CL}) 58, an comparator 60, and a logic block 62. Transistor 52 is typically a power MOSFET. Output current (Io) passing through transistor 52 also passes through Rs 54, since they are in series, and a voltage (Vs) develops across Rs 54. A current (I_{CL}) passing through constant current source 56 also passes through R_{CL} 58. When I_{CL} times R_{CL} equals Vs, the ungrounded input terminal of comparator 60 will be at zero volts. If Vs increases because Io increases, comparator 60 will act through logic block 62 to turn off transistor 52. If Vs decreases because Io decreases, comparator 60 will act through logic block 62 to turn on transistor 52. The net effect is to limit current. The point the current is limited to can easily be adjusted by varying the value of R_{CL} 58 or the current sourced by constant current source 56. Typical constant current values are 150–500 microamps. Values for RCL often range from 2K–10K ohms. The alternating current (AC) value of a sense current waveform is not affected when a current limit voltage is changed, because the current source develops a voltage across R_{CL} 58 which merely level shifts the sense voltage. In the prior art, attempts to scale the sense voltage also scale the AC waveform. A critical advantage is that a current input for controlling the current limit threshold allows for an easy implementation of a current mode controller using a simple current summing junction to combine multiple control inputs such as feedback, slope compensation, feed forward, soft start safety current limit, et cetera.

In FIG. 4, a second embodiment of the present invention is a voltage mode PWM controller power supply 70 comprising a high voltage switch 72 in series with the primary of a transformer 74 and a sense resistor (Rs) 76, a constant current source 78 in series with a resistor (RCL) 80, an comparator 82, a two-input AND-gate 84, a set-reset (SR) flip-flop 86, a PWM controller 88 having an oscillator 90. PWM controller 88 turns on the high voltage switch 72 every cycle of oscillator 90 by setting flip-flop 86.

In FIG. 5, a comparator 90, is an example of what can be used in place of op-amps 60 and 82, and comprises a comparator input 91 that is compared with the voltage on the emitter of a transistor 92 (here, ground). A pair of transistors 94 and 96 act as an emitter-follower in order to compensate for V_{be} in input transistor 92. A transistor 98 and a transistor 100 are constant current sources, the first delivering about 100 microamperes and the latter delivering fifty microamperes. Transistors 92, 94 and 96 are the same size transistors in order not to generate any offsets. A pair of transistors 102 and 104 guarantee that transistor 92 cannot saturate when the comparator input 91 goes HIGH. A transistor 106 is a relatively weak clamp that forces the collector of transistor 92 to stay short of rising completely to V_{dd}, in order to improve speed. A set of three inverters 107–109 provide additional gain and an appropriate output polarity.

In FIG. 6, a current mode controller 116, according to a fourth embodiment of the present invention, comprises a switch transistor 112, a transformer 114, a sense resistor (Rs) 136, a current limit control resistor 118, a current summing node 120 that receives a control current 122 and a current (Iref, typically 500 microamperes) from constant current source 124, a comparator 126, an oscillator 128, and a set-reset flip-flop 130. Control current 122 comprises a slope compensation (Isc), a soft start (Iss), a feed forward (Iff), and a feed back (Ifb, typically 0-500 microamperes) constituent currents. The current limit current (I_{CL}) flowing through resistor 118 is Iref-Ifb-Iff-Isc-Iss.

FIG. 7 shows a slope compensator 150 that derives its slope compensation from an OSC ramp and an external resistor input (RSLOPE) 151 to fix a current for subtraction from a summing junction Isc. Slope compensator 150 accepts the OSC ramp (typically a 0–1.75 volt sawtooth) at the base of a transistor 152 and the emitter of a transistor 154 after buffering. RSLOPE input 151 connects to the emitter of transistor 154. An external resistor 155 will set the slope compensation current. A resistor 156 provides the necessary bias currents for transistors 152 and 154. A pair of transistors 158 and 160 keep transistor 154 from saturating. A transistor 162 turns off the slope compensation ramp when an external high voltage switch transistor (e.g., transistor 112) turns off (MATCH goes HIGH). A resistor 170 and a transistor 172 soft clamp RSLOPE input 151 to about 2.75 volts. The soft clamp is needed for instances when RSLOPE input 151 is left open. If RSLOPE input 151 goes too high, a transistor 173 turns off, and an output 174 will go HIGH. A transistor 176 and a resistor 178 form a bias generator for the base of transistor 172 such that the gate of transistor 173 is 2.75 volts and transistor 173 is conducting (node 174 is LOW). A pair of transistors 180 and 182 convert the current reference from VS to GND. In the comparator, a transistor 184 sinks a fixed current of about twenty microamperes, and when transistor 173 turns on, that current will be overridden and the drain of transistor 184 will be forced HIGH. A group of transistors 186, 187, 188, and 190, and an inverter 192 are used in a power-down circuit. A resistor 194 and a capacitor 196 form a low pass filter so noise on the RSLOPE input 151, when left open, will not trigger the comparator into a LOW (50% mode). A pair of transistors 197 and 198 form an inverter to output 174.

FIG. 8 is a schematic diagram of a typical summing junction 200, such as is mentioned above in conjunction with FIG. 7. Summing junction 200 has a transistor 202 that sinks 480 microamperes from a feedback (FB) input with excess current passing through a transistor 204. A sixty microampere current in a transistor 206 is mir-

rored via a transistor 208 and multiplier by a factor of eight in transistor 202. A thirty microampere current in a transistor 214 is mirrored via a pair of transistors 216 and 218 and multiplied by eight. A transistor 220 lowers the effects of channel length modulation in transistor 214. Transistor 204 acts as a diode in prohibiting current flow from the emitter of a transistor 222 to the drain of transistor 202. Transistor 222, a transistor 224, and a resistor 226 buffer a relatively high impedance node "V" (at 1.25 volts) to a low impedance at the emitter of transistor 222. A transistor 228 mirrors to a transistor 230 a current resulting from subtracting currents FB, FP, and SUMJ from a 240 microampere current in transistor 218. Switching noise is prevented from getting to current reference "A" by a buffer comprising a current mirror transistor 240 (running at about fifteen microamperes) and a transistor 242 (running at about sixty microamperes). A transistor 246 matches the V_{gs} of transistor 230 in a parallel branch. A transistor 248 generates a bias voltage for a transistor 250 and transistor 252, which are cascode transistors. A plurality of transistors 251, 252, and 254 are input clamps and are not involved in the function of the summing function. A summing junction comparator (COMPSJ) 256 is described below in more detail.

FIG. 9 is a schematic diagram of a typical summing junction comparator 300, such as COMPSJ 256 (FIG. 8). Summing junction comparator 300 accepts a current reference signal APD which makes a transistor 302 conduct about thirty microamperes. This current is mirrored from a transistor 304 into a sixty microampere current in a transistor 306. A pair of transistors 308 and 310 form a cascode current reference for a plurality of transistors 312, 314, 316, 318, 320, and 321. Transistors 314 and 318 generate a 50% higher current than transistors 312 and 316 so that a positive offset can be created on an ILIMITC input. The offset is about 21 millivolts (2·10.5 mV). A pair of capacitors 322 and 324 suppress any noise on respective bias lines. A bootstrap circuit comprises transistors 321 and a transistor 326, a resistor 328, a capacitor 330, and a pair of transistors 332 and 334. Transistor 326 mirrors the thirty microampere current to transistor 332 via resistor 328. Capacitor 330 forces transistor 332 to turn on harder when the collector of a transistor 335 goes HIGH. More current is then forced through a transistor 336, speeding up the LOW to HIGH transitions of the comparator. A pair of transistors 338 and 340 keep transistor 335 from saturating. A pair of transistors 342 and 344 keep a transistor 346 out of saturation. The comparator input stage comprises the reference voltage stage with a pair of transistors 348 and 350 and a pair of input transistors 352 and 354. Each has its own current source. A second comparator stage has current source transistors 336 and 320 and transistor 335 together with a pair of transistors 360 and 362 that match the input stage in its configuration, transistor sizes, and current. Comparator 300 further comprises an output stage consisting of a transistor 364, a transistor 366, a transistor 368, and an inverter 370.

Comparator 300 delivers high speed at low levels of power consumption. Typical rise and fall times at 360 microamperes are about 25 nanoseconds. Comparator 300 comprises two reference current mirror stages, a reference voltage stage, and input and output stages. One of the current mirrors is used to set up a fixed current through the reference voltage stage and input stage. The other current mirror is such that bootstrapping is allowed so the LOW to HIGH transitions can be sped up. The input stage gets its reference voltage from the reference voltage stage which is matched with the input stage (in terms of the current ratios and the component sizes). A positive offset of twenty millivolts requires a 50% higher current to be forced through the reference voltage stage. The output stage has itself a three stage circuit where the first sub-stage current and components are matched to the input stage. The second and third sub-stages consist of one inverter each.

Although the present invention has been described in terms of the presently preferred embodiments, it is to be understood that the disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those skilled in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A system with current-limited output, the system comprising:

first and second power input terminals;

a system ground;

a sensing resistor between the second power input terminal and system ground;

first and second load terminals, the first load output terminal connected to the first power input terminal;

a comparator having a first and a second comparison input and a comparison output, said second comparison input connected to the system ground;

fixed voltage offset means for developing an offset voltage near ground potential from the second power input terminal when a current passing through the sensing resistor is at a control value and said offset voltage being applied to said first comparison input of the comparator;

a transistor having a drain connected to the second load output terminal, a source connected to the system ground, and a gate controlled by said comparison output of the comparator wherein a voltage developed across the sensing resistor is controlled to be substantially equal to said offset voltage.

2. The system of claim 1, wherein:

the fixed voltage offset means and sensing resistor are sized such that when a current flowing through the first and second load outputs reaches a predetermined level, the transistor may limit further increases.

3. The system of claim 1, further comprising:

logic means with an input connected to the comparator output and an output connected to said gate of the transistor for controlling said gate of the transistor.

4. The system of claim 3, wherein:

the logic means comprises an oscillator, a flip-flop, and a gate wherein said oscillator is coupled to said flip-flop and the transistor for controlling a current through the transistor by pulse width modulation of said gate.

5. A power supply, comprising:

positive and negative power input terminals;

a system ground;

a sensing resistor connected between the negative power input terminal and system ground;

first and second load output terminals, the first load output terminal connected to the positive power input terminal;

a comparator having a first and a second comparison input and a comparison output, said second comparison input connected to the system ground;

fixed voltage offset means for adding an offset voltage to a voltage at the negative power input terminal and for developing a positively-offset negative power input terminal voltage at said first comparison input of the comparator that is approximately equal to ground potential when a current passing through the sensing resistor is substantially equal to a level to be maintained by closed-loop servo control;

a power MOSFET switch transistor having a drain connected to the second load output terminal, a source connected to the system ground, and a gate controlled by said comparison output of the comparator.

6. The power supply of claim 5, further comprising:

a transformer with a primary winding connected to the first and second load output terminals.

7. A current mode controller, comprising:

a switching transistor;

a load transformer having a primary winding in series with the switching transistor;

a sense resistor in series with the switching transistor and a first input terminal for an external power source;

a current limit control resistor for connecting one end to said first input terminal;

a current summing node for receiving a reference current (Iref) from a constant current source and a control current including constituent currents for slope compensation (Isc), soft start (Iss), feed forward (Iff), and feedback (Ifb);

a set-reset flip-flop;

a comparator having a first input connected to the current summing node and a second input connected to a chip ground at a junction of the switching transistor and the sense resistor and an output for controlling the switching transistor by resetting the set-reset flip-flop; and

an oscillator for setting the set-reset flip-flop.

8. The controller of claim 7, further comprising:

reference current means for generating said reference current (Iref) of approximately 500 microamperes;

slope compensation means for generating said slope compensation current (Isc);

soft start means for generating said soft start current (Iss) wherein current initially deliverable by the controller has a safety limit;

feed forward means for generating said feed forward current (Iff) for control loop compensation for changes in input voltage; and

feedback means for generating said feedback current (Ifb) in the range of 0-500 microamperes for providing a closed-loop servo control of the controller.

* * * * *

DX 1001

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DX 1002

REDACTED

DX 1003

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DX 1004

POWER INTEGRATIONS INC

FORM 10-Q
(Quarterly Report)

Filed 11/7/2005 For Period Ending 9/30/2005

Address	5245 HELLYER AVE
	SAN JOSE, California 95138
Telephone	408-414-9200
CIK	0000833640
Industry	Semiconductors
Sector	Technology
Fiscal Year	12/31

EXHIBIT
BALAKRISHNAN
42
3-15-06

Case No. 04-1371-JJF
DEFT Exhibit No. DX 1004
Date Entered _____
Signature _____

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, D.C. 20549

FORM 10-Q

(Mark One)

☒ QUARTERLY REPORT UNDER SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

FOR THE QUARTERLY PERIOD ENDED September 30, 2005

☐ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

FOR THE TRANSITION PERIOD FROM TO

COMMISSION FILE NUMBER: 0-23441

POWER INTEGRATIONS, INC.
(EXACT NAME OF REGISTRANT AS SPECIFIED IN ITS CHARTER)

DELAWARE	94-3065014
(State of Incorporation)	(I.R.S. Employer Identification No.)

5245 Hellyer Avenue, San Jose, California 95138
(Address of principal executive offices) (Zip Code)

(408) 414-9200
(Registrant's telephone number, including area code)

(Former name, former address and former fiscal year, if changed since last report)

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to the filing requirements for the past 90 days. Yes ☒ No ☐

Indicate by check mark whether the registrant is an accelerated filer (as defined in Rule 12b-2 of the Exchange Act). Yes ☒ No ☐

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). ☐ Yes ☒ No

APPLICABLE ONLY TO ISSUERS INVOLVED IN BANKRUPTCY PROCEEDINGS DURING THE PRECEDING FIVE YEARS

Indicate by check mark whether the registrant has filed all documents and reports required to be filed by Sections 12, 13 or 15(d)of the Securities Exchange Act of 1934 subsequent to the distribution of securities under a plan confirmed by a court. ☐ Yes ☐ No

APPLICABLE ONLY TO CORPORATE ISSUERS:

Indicate the number of shares outstanding of each of the issuer's classes of common stock, as of the latest practicable date.

Class / Common Stock, $.001 par value	Outstanding at October 31, 2005 / 29,548,096 shares

POWER INTEGRATIONS, INC.

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PART I. FINANCIAL INFORMATION

ITEM 1. CONDENSED CONSOLIDATED FINANCIAL STATEMENTS

POWER INTEGRATIONS, INC.

CONDENSED CONSOLIDATED BALANCE SHEETS
(unaudited)
(In thousands)

	September 30, 2005	December 31, 2004
ASSETS		
CURRENT ASSETS:		
Cash and cash equivalents	$ 100,143	$ 108,596
Short-term investments	14,738	2,750
Accounts receivable	12,242	12,230
Inventories	22,300	25,354
Deferred tax assets	4,024	3,678
Prepaid expenses and other current assets	1,264	2,600
Total current assets	157,216	155,208
PROPERTY AND EQUIPMENT, net	49,615	51,718
INVESTMENTS	6,958	7,451
DEFERRED TAX ASSETS	1,789	1,923
OTHER ASSETS	13,812	11,152
	$ 229,590	$ 235,452
LIABILITIES AND STOCKHOLDERS' EQUITY		
CURRENT LIABILITIES:		
Accounts payable	$ 6,635	$ 5,612
Accrued payroll and related expenses	4,180	4,672
Income taxes payable	5,459	5,698
Deferred income on sales to distributors	3,002	3,058
Other accrued liabilities	2,672	2,480
Total current liabilities	21,948	21,520
STOCKHOLDERS' EQUITY:		
Common stock	30	30
Additional paid-in capital	102,578	122,895
Cumulative translation adjustment	(114)	(114)
Retained earnings	105,148	89,701
Total stockholders' equity	207,642	213,512
	$ 229,590	$ 235,452

The accompanying notes are an integral part of these condensed consolidated financial statements.

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POWER INTEGRATIONS, INC.

CONDENSED CONSOLIDATED STATEMENTS OF INCOME
(unaudited)
(In thousands, except per share amounts)

	Three Months Ended September 30,		Nine Months Ended September 30,	
	2005	2004	2005	2004
NET REVENUES	$36,543	$32,946	$106,258	$105,055
COST OF REVENUES	18,463	17,188	54,287	54,053
GROSS PROFIT	18,080	15,758	51,971	51,002
OPERATING EXPENSES				
Research and development	4,105	4,096	12,307	12,336
Sales and marketing	4,418	3,912	12,699	11,461
General and administrative	4,092	2,382	9,802	6,010
Total operating expenses	12,615	9,890	34,808	29,807
INCOME FROM OPERATIONS	5,465	5,868	17,163	21,195
OTHER INCOME, net	939	339	2,318	729
INCOME BEFORE PROVISION FOR INCOME TAXES	6,404	6,207	19,481	21,924
PROVISION FOR INCOME TAXES	739	502	4,034	4,067
NET INCOME	$5,665	$5,705	$15,447	$17,857
EARNINGS PER SHARE				
Basic	$ 0.19	$ 0.18	$ 0.52	$ 0.58
Diluted	$ 0.18	$ 0.18	$ 0.50	$ 0.55
SHARES USED IN PER SHARE CALCULATION				
Basic	29,478	30,912	29,605	30,774
Diluted	30,742	31,994	30,760	32,506

The accompanying notes are an integral part of these condensed consolidated financial statements.

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POWER INTEGRATIONS, INC.

CONDENSED CONSOLIDATED STATEMENTS OF CASH FLOWS
(unaudited)
(In thousands)

	Nine Months Ended September 30,	
	2005	2004
CASH FLOWS FROM OPERATING ACTIVITIES		
Net income	$ 15,447	$ 15,851
Adjustments to reconcile net income to net cash provided by operating activities:		
Depreciation and amortization	4,930	5,161
Deferred income taxes	(10)	—
Provision for (reduction in) accounts receivable and other allowances	76	380
Income tax benefit associated with employee stock plans	1,007	2,119
Stock compensation to non-employees	8	31
Change in operating assets and liabilities:		
Accounts receivable	(2,595)	329
Inventories	3,054	894
Prepaid expenses and other current assets	1,298	(757)
Accounts payable	(2,242)	(892)
Income taxes payable and accrued liabilities	1,061	512
Deferred income on sales to distributors	(56)	1,015
Net cash provided by operating activities	21,978	25,136
CASH FLOWS FROM INVESTING ACTIVITIES		
Purchases of property and equipment	(2,270)	(4,245)
Acquisition of technology, patents / licenses	(1,094)	(310)
Note to supplier	(10,000)	—
Purchases of held-to-maturity investments	(6,806)	(63,895)
Proceeds from maturities of held-to-maturity investments	11,271	46,585
Net cash used in investing activities	(8,899)	(21,865)
CASH FLOWS FROM FINANCING ACTIVITIES		
Net proceeds from issuance of common stock	6,973	7,926
Repurchase of common stock	(28,305)	—
Principal payments under capitalized lease obligations	—	(41)
Net cash (used in) provided by financing activities	(21,332)	7,885
NET (DECREASE) INCREASE IN CASH AND CASH EQUIVALENTS	(8,253)	11,156
CASH AND CASH EQUIVALENTS AT BEGINNING OF PERIOD	108,396	92,045
CASH AND CASH EQUIVALENTS AT END OF PERIOD	$100,143	$103,201
SUPPLEMENTAL DISCLOSURE OF NON-CASH INVESTING AND FINANCING ACTIVITIES		
Unpaid property and equipment	$ 265	$ 463
SUPPLEMENTAL DISCLOSURE OF CASH FLOW INFORMATION		
Cash paid for income taxes, net	$ 3,320	$ 268

The accompanying notes are an integral part of these condensed consolidated financial statements.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS

(Unaudited)

1. BASIS OF PRESENTATION:

The condensed consolidated financial statements include the accounts of Power Integrations, Inc., a Delaware corporation and its wholly owned subsidiaries (the "Company"). Significant inter-company accounts and transactions have been eliminated.

While the financial information furnished is unaudited, the condensed consolidated financial statements included in this report reflect all adjustments (consisting only of normal recurring adjustments) which the Company considers necessary for the fair presentation of the results of operations for the interim periods covered and the financial condition of the Company at the date of the interim balance sheet. The results for interim periods are not necessarily indicative of the results for the entire year. Certain reclassifications were made to the prior year financial information to conform to the current period presentation. The condensed consolidated financial statements should be read in conjunction with the Company's consolidated financial statements and the notes thereto for the year ended December 31, 2004 included in its Form 10-K filed on March 16, 2005 with the Securities and Exchange Commission.

Reclassifications

In the accompanying condensed consolidated balance sheet as of December 31, 2004, the Company has reclassified the balance of auction rate securities (for which interest rates reset in less than 90 days, but for which the underlying maturity date is longer than 90 days), from cash and cash equivalents to long-term investments. This resulted in the reclassification from cash and cash equivalents to long-term investments of approximately $11.2 million as of December 31, 2004. Also, in connection with this reclassification, there was a corresponding net increase in cash used in investing activities in the accompanying condensed consolidated statements of cash flows by approximately $10.0 million for the nine month period ended September 30, 2004 to reflect the purchase of these investments during that period. The Company had no auction rate securities at September 30, 2005.

2. SUMMARY OF SIGNIFICANT ACCOUNTING POLICIES:

Cash and Cash Equivalents and Short-Term and Long-Term Investments

The Company considers cash invested in highly liquid financial instruments with a remaining maturity of three months or less at the date of purchase to be cash equivalents. Investments in highly liquid financial instruments with maturities greater than three months but not longer than twelve months from the balance sheet date are classified as short-term investments. Investments in highly liquid financial instruments with maturities greater than twelve months from the balance sheet date are classified as long-term investments. As of September 30, 2005, the Company's short-term and long-term investments consisted of U.S. government-backed securities, municipal bonds, corporate commercial paper and other high-quality commercial securities, which were classified as held-to-maturity and were valued using the amortized cost method, which approximates fair market value.

Revenue Recognition

Revenues consist of sales to original equipment manufacturers, or OEMs, merchant power supply manufacturers and distributors. Shipping terms to international OEMs and merchant power supply manufacturers are delivered at frontier, which is commonly referred to as DAF. As such, title to the product passes to the customer when the shipment reaches the destination country and revenue is recognized upon the arrival of the Company's product in that country. Revenue from sales to North American OEMs and merchant power supply manufacturers are recognized upon shipment (FOB-point of origin), as this is when the title is passed to the customer.

Sales to distributors are made under terms allowing certain rights of return and protection against subsequent price declines on the Company's products held by the distributors. As a result of the Company's distributor agreements, the Company defers the recognition of revenue and the costs of revenues derived from sales to distributors until such distributors resell the Company's products to their customers. The Company determines the amounts to defer based on the level of actual inventory on hand at its distributors as well as inventory that is in transit to its distributors. The gross profit that is deferred as a result of this policy is reflected as "deferred income on sales to distributors" in the accompanying condensed consolidated balance sheet.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

Expense related to employee ownership programs through stock options

The Company has elected to follow Accounting Principles Board Opinion (APB) No. 25, *Accounting for Stock Issued to Employees* , and related interpretations, in accounting for employee stock options rather than the alternative fair value accounting allowed by SFAS No. 123, *Accounting for Stock Based Compensation* . APB No. 25 provides that expense relative to the Company's employee ownership programs through stock options is measured based on the intrinsic value of stock options granted on the date of the grant and the Company recognizes expense in its statement of income using the straight-line method over the vesting period for fixed awards. Under SFAS No. 123, the fair value of stock options at the date of grant is recognized in earnings over the vesting period of the options. Had expense related to employee ownership programs through the Company's stock option plans been determined under a fair value method consistent with SFAS No. 123, *Accounting for Stock Based Compensation* , and related interpretations, the Company's net income would have been reduced to the following pro forma amounts (in thousands, except per share information):

	Three Months Ended September 30,		Nine Months Ended September 30,	
	2005	2004	2005	2004
Net income, as reported	$5,665	$5,705	$15,447	$15,851
Deduct: Total stock-based employee stock ownership expense determined under fair-value-based method for all awards, net of tax:				
Stock options granted under stock option plans	(4,860)	(4,161)	(13,431)	(13,660)
Stock purchase rights under the Employee Purchase Plan	(57)	(138)	(373)	(460)
Pro forma net income	$748	$1,406	$1,643	$1,731
Basic earnings per share:				
As reported	$0.19	$0.18	$0.52	$0.52
Pro forma	$0.03	$0.05	$0.05	$0.06
Diluted earnings per share:				
As reported	$0.18	$0.18	$0.50	$0.49
Pro forma	$0.02	$0.04	$0.05	$0.05

The fair value of stock options granted is established on the date of the grant using the Black-Scholes option pricing model with the following weighted average assumptions:

	Three Months Ended September 30,		Nine Months Ended September 30,	
	2005	2004	2005	2004
Risk-free interest rates	3.76%	3.54%	3.39%	2.99% - 3.54%
Expected volatility rates	66%	78%	66%	78%
Expected dividend yield				
Expected life of stock options (years)	4.59	5.20	4.59	5.20
Weighted-average grant-date fair value of options granted	$22.50	$19.26	$18.09	$26.46

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

The fair value of employees' stock purchase rights under the Company's employee stock purchase plan was estimated using the Black-Scholes model with the following weighted average assumptions:

	Three Months Ended September 30,		Nine Months Ended September 30,	
	2005	2004	2005	2004
Risk-free interest rates	3.44%	1.79%	3.44%	1.00% - 1.79%
Expected volatility rates	34%	54%	34%	54%
Expected dividend yield				
Expected life (years)	0.5	0.5	0.5	0.5
Weighted-average estimated fair value of purchase rights	$15.94	$17.28	$15.94	$17.28

Common Stock

On October 20, 2004, the Company announced that its board of directors had authorized the repurchase of up to $40.0 million of the Company's common stock. The board directed that the repurchases be made pursuant to Rule 10b5-1 of the Exchange Act. From inception of the stock repurchase program in October 2004 through June 30, 2005, the Company repurchased 2,033,270 shares for approximately $40.0 million, the total amount authorized by the Company's board of directors. The Company repurchased 373,270 shares for approximately $8.1 million during the three months ended June 30, 2005, and 1.1 million shares for approximately $20.2 million during the three months ended March 31, 2005. On October 19, 2005, the Company announced that its board of directors had authorized a second stock repurchase program of up to $25.0 million of the Company's common stock. The board directed that the repurchases be made pursuant to Rule 10b5-1 of the Exchange Act. The repurchases will take place from time to time on the open market.

Use of Estimates

The preparation of financial statements in conformity with accounting principles generally accepted in the United States of America requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosures of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the reporting period. Actual results could differ from those estimates. On an on-going basis, the Company evaluates its estimates, including those related to revenue recognition and allowances for receivables and inventories. These estimates are based on historical facts and various other assumptions that the Company believes to be reasonable at the time the estimates are made.

Comprehensive Income

Comprehensive income for the Company consists of net income, plus the effect of foreign currency translation adjustments. Such adjustments were not material for the nine months ended September 30, 2005 and 2004. Accordingly, comprehensive income closely approximates actual net income.

Segment Reporting

The Company is organized and operates as one business segment - the design, development, manufacture and marketing of proprietary, high-voltage, analog integrated circuits for use primarily in the AC-to-DC and DC-to-DC power conversion markets. The Company's chief operating decision maker, the Chief Executive Officer, reviews financial information presented on a consolidated basis for purposes of making operating decisions and assessing financial performance.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

3. INVENTORIES:

Inventories are stated at the lower of cost (first-in, first-out) or market and consist of the following (in thousands):

	September 30, 2005	December 31, 2004
Raw materials	$ 2,616	$ 1,976
Work-in-process	6,630	7,212
Finished goods	13,054	16,766
	$ 22,300	$ 25,954

4. SIGNIFICANT CUSTOMERS AND EXPORT SALES:

Customer Concentration

The Company's end user base is highly concentrated and a relatively small number of OEMs, power supply merchants and distributors typically account for a significant portion of the Company's net revenues. Ten customers accounted for approximately 69.0% and 69.9% of total net revenues for the three months ended September 30, 2005 and 2004, respectively, and 69.7% and 70.4% of total net revenues for the nine months ended September 30, 2005 and 2004, respectively.

The following customers accounted for more than 10% of total net revenues:

	Three Months Ended September 30,		Nine Months Ended September 30,	
Customer	2005	2004	2005	2004
A	9.7%	15.2%	10.4%	13.3%
B	18.1%	17.4%	17.3%	17.0%
C	*	*	*	10.7%

* less than 10%

Customers A and B are distributors of the Company's products and customer C is an OEM.

Concentration of Credit Risk

Financial instruments that potentially subject the Company to concentrations of credit risk consist principally of cash investments and trade receivables. The Company has cash investment policies that limit cash investments to low risk investments. With respect to trade receivables, the Company performs ongoing credit evaluations of its customers' financial condition and requires letters of credit whenever deemed necessary. Additionally, the Company establishes an allowance for doubtful accounts based upon factors surrounding the credit risk of specific customers, historical trends related to past losses and other relevant information. Account balances are charged off against the allowance after all means of collection have been exhausted and the potential for recovery is considered remote. The Company does not have any off-balance sheet credit exposure related to its customers. As of September 30, 2005 and December 31, 2004, approximately 70.4% and 81.9% of accounts receivable, respectively, were concentrated with the top ten customers.

The following customers accounted for more than 10% of accounts receivable:

Customer	September 30, 2005	December 31, 2004
A	20.1%	29.0%
B	17.9%	26.1%

Customers A and B are distributors of the Company's products.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

Export Sales

The Company markets its products in North America and in foreign countries through its sales personnel and a worldwide network of independent sales representatives and distributors. As a percentage of total net revenues, export sales, which consist of domestic and foreign sales to customers in foreign countries, are comprised of the following:

	Three Months Ended September 30,		Nine Months Ended September 30,	
	2005	2004	2005	2004
Taiwan	26.9%	24.1%	25.7%	28.3%
Hong Kong/China	23.5%	24.4%	24.1%	26.9%
Korea	18.9%	18.5%	19.9%	20.6%
Western Europe (excluding Germany)	11.7%	12.7%	10.9%	10.2%
Germany	4.0%	5.1%	4.0%	4.5%
Japan	3.6%	2.1%	3.7%	2.5%
Singapore	2.8%	3.7%	2.7%	1.9%
Other	1.6%	2.6%	1.7%	2.5%
Total foreign	93.0%	91.2%	92.9%	91.8%

Product Sales

Sales of the Company's TOPSwitch and TinySwitch products accounted for 93.7% and 97.8% of net revenues from product sales for the three months ended September 30, 2005 and 2004, respectively, and 95.2 % and 97.3% of net revenues from product sales for the nine months ended September 30, 2005 and 2004, respectively. TOPSwitch products include TOPSwitch, TOPSwitch-II, TOPSwitch-FX and TOPSwitch-GX. TinySwitch products include TinySwitch and TinySwitch II.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

5. EARNINGS PER SHARE:

Basic earnings per share are calculated by dividing net income by the weighted average shares of common stock outstanding during the period. Diluted earnings per share are calculated by dividing net income by the weighted average shares of common stock and dilutive common equivalent shares outstanding during the period. Dilutive common equivalent shares included in the diluted calculation consists of shares issuable upon the exercise of outstanding common stock options computed using the treasury stock method.

A summary of the earnings per share calculation is as follows (in thousands, except per share amounts):

	Three Months Ended September 30,		Nine Months Ended September 30,	
	2005	2004	2005	2004
Basic earnings per share:				
Net income	$ 5,665	$ 5,705	$15,447	$15,851
Weighted average common shares	29,473	30,912	29,605	30,774
Basic earnings per share	$ 0.19	$ 0.18	$ 0.52	$ 0.52
Diluted earnings per share:				
Net income	$ 5,665	$ 5,705	$15,447	$15,851
Weighted average common shares	29,473	30,912	29,605	30,774
Effect of dilutive securities:				
Stock options	1,245	1,070	1,136	1,684
Employee stock purchase plan	9	12	19	43
Diluted weighted average common shares	30,732	31,994	30,760	32,501
Diluted earnings per share	$ 0.18	$ 0.18	$ 0.50	$ 0.49

Options to purchase 3,667,374 and 2,021,238 shares of the Company's common stock outstanding for the three month periods ended September 30, 2005 and 2004, respectively, and options to purchase 3,592,841 and 1,537,701 shares of the Company's common stock outstanding for the nine month periods ended September 30, 2005 and 2004, respectively, were not included in the computation of diluted earnings per share for the periods then ended because the exercise prices of the options to purchase shares of Company common stock were greater than the average market price of the Company's common stock during those periods, and therefore, their effect would have been antidilutive.

6. PROVISION FOR INCOME TAXES:

Income tax expense for the nine-month periods ended September 30, 2005 and 2004 includes a provision for Federal, state and foreign taxes based on the annual estimated effective tax rate applicable to the Company and its subsidiaries. The difference between the Federal statutory rate of 35% and the Company's effective tax rate used for the nine-month period ended September 30, 2005 and 2004 is primarily due to the beneficial impact of international sales subject to lower tax rates, as well as research and development tax credits. The Company adjusted its effective tax rate from 25% at June 30, 2005 to 21% for the nine months ended September 30, 2005 to reflect the estimated annual effective income tax rate for 2005. The change in the estimated effective tax rate for 2005 resulted in an effective tax rate of 12% for the three months ended September 30, 2005. The tax provision for the three and nine month periods ended September 30, 2004 was calculated using an annual effective income tax rate of 26%, which was adjusted for the favorable conclusion of certain tax contingencies in the third quarter of 2004, which resulted in an effective tax rate of approximately 8% and 20% for the three and nine month periods, respectively. The estimated annual effective income tax rate for 2005 may be subject to change in the future.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

The American Jobs Creation Act of 2004 (the Jobs Act), enacted on October 22, 2004, provides for a special one-time tax deduction of 85 percent of certain foreign earnings that are repatriated. The deduction would result in an approximate 5.25% Federal tax rate on the repatriated earnings. To qualify for the deduction, the earnings must be reinvested in the United States pursuant to a domestic reinvestment plan established by the company's chief executive officer and approved by the company's board of directors. Certain other criteria in the Jobs Act must be satisfied as well.

The Company is currently analyzing the impact of the one-time favorable foreign dividend provision recently enacted as part of the Jobs Act, and intends to complete the analysis by the end of fiscal year 2005. As of September 30, 2005, and based on the tax laws in effect at that time, the Company intends to continue to indefinitely reinvest the Company's undistributed foreign earnings and accordingly, no deferred tax liability has been recorded on these undistributed foreign earnings.

7. INDEMNIFICATIONS:

The Company sells products to its distributors under contracts, collectively referred to as Distributor Sales Agreements (DSA). Each DSA contains the relevant terms of the contractual arrangement with the distributor, and generally includes certain provisions for indemnifying the distributor against losses, expenses, and liabilities from damages that may be awarded against the distributor in the event the Company's hardware is found to infringe upon a patent, copyright, trademark, or other proprietary right of a third party (Customer Indemnification). The DSA generally limits the scope of and remedies for the Customer Indemnification obligations in a variety of industry-standard respects, including, but not limited to, limitations based on time and geography, and a right to replace an infringing product. The Company also, from time to time, has granted a specific indemnification to individual customers.

The Company believes its internal development processes and other policies and practices limit its exposure related to such indemnifications. In addition, the Company requires its employees to sign a proprietary information and inventions agreement, which assigns the rights to its employees' development work to the Company. To date, the Company has not had to reimburse any of its distributors or customers for any losses related to these indemnifications and no material claims were outstanding as of September 30, 2005. For several reasons, including the lack of prior indemnification claims and the lack of a monetary liability limit for certain infringement cases, the Company cannot determine the maximum amount of potential future payments, if any, related to such indemnifications.

8. COMMITMENTS AND CONTINGENCIES

From time to time in the ordinary course of business the Company could become involved in lawsuits, or customers and distributors may make claims against the Company. During 2004, a small number of product lots of one of the Company's products were not built to design specifications because of a foundry process defect. As a result of this manufacturing defect, there were a limited number of product failures and the Company replaced all of the parts that had not yet been installed in end-customer products. Several customers made requests for reimbursement of costs and expenses in excess of the Company's contractual warranty liability. In accordance with SFAS No. 5, *Accounting for Contingencies* , the Company makes a provision for a liability when it is both probable that a liability has been incurred and the amount of the loss can be reasonably estimated. After further discussions with its customers, the Company determined that it was appropriate to accrue approximately $90,000 in the three months ended September 30, 2005, and a total of approximately $481,000 in the nine months ended September 30, 2005, related to this manufacturing defect, for customer costs and expenses in excess of the Company's contractual warranty liability. The Company expects that there will be no additional charges related to this matter.

9. LEGAL PROCEEDINGS:

On June 28, 2004, the Company filed a complaint for patent infringement in the U.S. District Court, Northern District of California, against System General Corporation, a Taiwanese company and its U.S. subsidiary. The Company's complaint alleges that certain integrated circuits produced by System General Corporation infringed and continue to infringe certain of the Company's patents. The Company seeks, among other things, an order enjoining System General Corporation from infringing the Company's patents and an award for damages resulting from the alleged infringement.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

On May 9, 2005, the Company filed a complaint with the U.S. International Trade Commission (ITC) under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. section 1337, naming System General Corporation of Taiwan as the respondent. The Company filed a supplement to the complaint on May 24, 2005. The Company alleges infringement by System General of the same patents raised in the action in the Northern District of California. The ITC instituted an investigation on June 8, 2005 in response to the Company's complaint. By its complaint, the Company seeks an order from the ITC excluding System General's PWM chips and the products containing them, such as LCD monitors, from importation into the United States. The ITC hearing is scheduled to begin on January 18, 2006, based on the hearing, the judge will make an initial determination of weather System General is infringing the Company's patents. On June 10, 2005, in response to the initiation of the ITC investigation, the District Court stayed all proceedings.

On October 20, 2004, the Company filed a complaint for patent infringement in the U.S. District Court for the District of Delaware, against Fairchild Semiconductor International, Inc., a Delaware corporation, and Fairchild Semiconductor Corporation, a Delaware corporation (collectively, Fairchild). The Company's complaint alleges that Fairchild produces certain integrated circuits, which infringed and continue to infringe certain of the Company's patents. The Company seeks, among other things, an order enjoining Fairchild from infringing the Company's patents and an award for damages resulting from the alleged infringement.

There can be no assurance that the Company will prevail in its litigation with either System General or Fairchild. This litigation, whether or not determined in the Company's favor or settled by the Company, will be costly and will divert the efforts and attention of the Company's management and technical personnel from normal business operations, which could have a material adverse effect on the Company's business, financial condition and operating results. Adverse determinations in litigation could result in the loss of the Company's proprietary rights, subject the Company to significant liabilities, require the Company to seek licenses from third parties or prevent the Company from licensing its technology, any of which could have a material adverse effect on the Company's business, financial condition and operating results.

10. CUMULATIVE ADJUSTMENT TO DEFERRED INCOME ON SALES TO DISTRIBUTORS

During the three months ended March 31, 2005, the Company made a change to its method of calculating deferred income on sales to distributors. This change resulted in the recognition of $1.1 million in previously deferred revenue, the recognition of $0.6 million of previously deferred costs, and an increase in net income of approximately $0.4 million, which represented diluted earnings per share of approximately $0.01. The impact of this adjustment was not material to any of the Company's prior period financial statements. The Company made no additional adjustments related to the change in the Company's method of calculating deferred income on sales to distributors in the three months ended September 30, 2005.

11. ADJUSTMENT TO RESERVE FOR SALES RETURNS

To estimate sales returns and allowances, the Company analyzes the reserve each quarter. When the Company reviews the adequacy of the reserve, the following factors are considered: historical returns, current economic trends, levels of inventories of the Company's products held by the Company's customers, and changes in customer demand and acceptance of our products. In the three months ended June 30, 2005, the Company made an adjustment to its sales returns reserve. The Company determined that it should have recorded this adjustment in prior periods. This adjustment increased net revenue and net income by approximately $0.9 million and approximately $0.4 million (or $0.01 per diluted share), respectively, for the three and six months ended June 30, 2005. This adjustment was not material to any of the Company's quarterly or annual periods.

12. LOAN TO SUPPLIER

On August 30, 2005, the Company entered into a loan agreement with one of its suppliers to fund their working capital needs. The principal amount of the loan was $10.0 million. The unpaid principal and interest is due on December 31, 2009. The loan is convertible into equity of the supplier upon certain conditions at the discretion of the Company. The interest rate will follow the one-year Treasury bill rate, and be reset at each anniversary of the closing date of the loan agreement. The loan principal is reflected in "Other Assets" in the accompanying 2005 condensed consolidated balance sheet.

POWER INTEGRATIONS, INC.

NOTES TO CONDENSED CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

13. RECENT ACCOUNTING PRONOUNCEMENTS:

In December 2004, the FASB issued FASB Staff Position No.109-1 (FAS 109-1), *Application of FASB Statement No.109, Accounting for Income Taxes, to the Tax Deduction on Qualified Production Activities Provided by the American Jobs Creation Act of 2004* (the AJCA). The AJCA introduces a special 9% tax deduction on qualified production activities. FAS 109-1 clarifies that this tax deduction should be accounted for as a special tax deduction in accordance with Statement 109. The Company is currently evaluating the impact of FAS 109-1, however the Company does not believe it will have a material impact on the Company's financial statements.

In December 2004, the Financial Accounting Standards Board (FASB) issued Statement of Financial Accounting Standards (SFAS) No. 123 (revised 2004) *Share-Based Payment* (SFAS 123R), which replaces SFAS No. 123 *Accounting for Stock-Based Compensation* (SFAS 123) and supersedes APB Opinion No. 25 *Accounting for Stock Issued to Employees* . The pro forma disclosures previously permitted under SFAS 123 no longer will be an alternative to financial statement recognition. Under SFAS 123(R), beginning January 1, 2006, the Company must determine the appropriate fair value model to be used for valuing share-based payments, the amortization method for compensation cost and the transition method to be used at the date of adoption. The transition methods include a modified-prospective and a modified-retroactive adoption options. Under the modified-retroactive option, prior periods may be restated either as of the beginning of the year of adoption or for all periods presented. The modified-prospective method requires that compensation expense be recorded for all unvested stock options and restricted stock at the beginning of the first quarter of adoption of SFAS 123(R), while the modified-retroactive methods would record compensation expense for all unvested stock options and restricted stock beginning with the first period restated. The Company is evaluating the requirements of SFAS 123(R), and expects that the adoption of SFAS 123(R) will have a material impact on its consolidated results of operations and earnings per share. The Company has decided to use the Black-Scholes closed-form model valuation technique to value its share options, and it has not been determined whether the valuation method adopted will result in amounts that are similar to the current pro forma disclosures under SFAS 123.

In March 2005, the SEC issued Staff Accounting Bulletin 107 (SAB 107), *Share-Based Payment* , which expresses views of the SEC staff regarding the application of SFAS No. 123(R). Among other things, SAB 107 provides interpretive guidance related to the interaction between SFAS No. 123(R) and certain SEC rules and regulations, as well as the SEC staff's views regarding the valuation of share-based payment arrangements for public companies.

In March 2005, the FASB issued FSP No. 46(R)-5, *Implicit Variable Interests under FASB Interpretation No. 46 (revised December 2003), Consolidation of Variable Interest Entities* (FSP 46(R)-5), which provides guidance for a reporting enterprise on whether it holds an implicit variable interest in a variable interest entity (VIE) or potential VIE when specific conditions exist. FSP 46(R)-5 became applicable to the Company in the quarter ended June 30, 2005. FSP 46(R) had no impact on the Company's consolidated results of operations and financial condition as of September 30, 2005.

In March 2005, the FASB issued FIN 47, *Accounting for Conditional Asset Retirement Obligations, an interpretation of FASB Statement No. 143* (FIN 47), which requires an entity to recognize a liability for the fair value of a conditional asset retirement obligation when incurred if the liability's fair value can be reasonably estimated. FIN 47 is effective for fiscal years ending after December 15, 2005. The Company is currently evaluating the effect that the adoption of FIN 47 will have on the Company's consolidated results of operations and financial condition, but does not expect it to have a material impact.

In May 2005, the FASB issued SFAS No. 154, *Accounting Changes and Error Corrections* (SFAS 154) that replaces Accounting Principles Board Opinions No. 20 *Accounting Changes* and SFAS No. 3, *Reporting Accounting Changes in Interim Financial Statements—An Amendment of APB Opinion No. 28* . SFAS 154 provides guidance on the accounting for and reporting of accounting changes and error corrections. It establishes retrospective application, or the latest practicable date, as the required method for reporting a change in accounting principle and the reporting of a correction of an error. SFAS 154 is effective for accounting changes and corrections of errors made in fiscal years beginning after December 15, 2005 and is required to be adopted by the Company in the first quarter of fiscal 2006. The Company is currently evaluating the effect that the adoption of SFAS 154 will have on the Company's consolidated results of operations and financial condition, but does not expect it to have a material impact.

ITEM 2. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS.

This Management's Discussion and Analysis of Financial Condition and Results of Operations includes a number of forward-looking statements, which reflect our current views with respect to future events and financial performance. In this report, the words "will", "expects", "believe", "should", "anticipate", "if", "future" and similar expressions identify forward-looking statements. Such statements are subject to certain risks and uncertainties, including our development efforts, the success of our product strategies, the maintenance of significant business relationships, as well as those discussed in the "Factors That May Affect Future Results of Operations" and elsewhere in this report. As a result of these risks, our actual results may differ materially from our historical or anticipated results. We caution you not to place undue reliance on these forward-looking statements, which speak only as of the date of this report.

The following management's discussion and analysis of financial condition and results of operations should be read in conjunction with management's discussion and analysis of financial condition and results of operations included in our Form 10-K for the year ended December 31, 2004.

Overview

We design, develop, manufacture and market proprietary high-voltage analog integrated circuits, commonly referred to as ICs, primarily for use in electronic power supplies, also known as switched-mode power supplies or switchers. Power supplies convert electricity from a source, such as a wall socket, to the power needed by an electronic device. This conversion entails, among other functions, reducing the voltage and, when necessary, converting alternating current to direct current (AC-DC). Switched-mode power supplies perform these functions using an array of electronic components, often including ICs such as ours. The vast majority of our ICs are used in AC-DC switchers, though we are now also targeting certain DC-DC applications such as power-over-Ethernet devices. Our focus is on applications that are sensitive to size, portability, energy efficiency and time-to-market, which are the primary benefits that our ICs provide. We have targeted applications in the following markets for our ICs:

the communications market;

the consumer market;

the computer market; and

the industrial electronics markets.

We believe that our patented TOPSwitch ICs, introduced in 1994, were the first highly integrated power conversion ICs to achieve widespread market acceptance. Since the introduction of TOPSwitch, we have introduced a number of other families of AC-DC switcher ICs, including TinySwitch and LinkSwitch, that further improve upon the functionality and cost-effectiveness of TOPSwitch, and enable us to address a wider range of applications. In June 2002, we further expanded our addressable market with the introduction of DPA-Switch, a highly integrated high-voltage DC-DC power conversion IC designed specifically for use in distributed power architectures. In October 2005, we introduced LinkSwitch-LP, which was specifically designed to replace unregulated linear transformers that are typically used in very low-powered applications. With our current portfolio of product families, we can address applications requiring up to 290 watts of power, in AC-DC applications, and up to 100 watts of power in DC-DC applications.

Our quarterly operating results are volatile and difficult to predict. Our net revenues and operating results have varied significantly in the past, are difficult to forecast and are subject to numerous factors both within and outside of our control. As a result, our quarterly and annual operating results may fluctuate significantly in the future. For a discussion of the factors that may affect our quarterly and annual operating results, please see "Factors that May Affect Future Results of Operations."

A portion of our cost of revenues consists of the cost of wafers. We currently purchase wafers from Matsushita Electric Industrial Co, Ltd. (Matsushita), OKI Electric Industry (OKI), and ZMD Analog Mixed Signal Services GmbH & CoKG (ZMD). In July 2005, we signed a new wafer supply agreement with Matsushita. The contract prices to purchase wafers from Matsushita and OKI are denominated in Japanese yen. The agreements with these vendors allow for mutual sharing of the impact of the exchange rate fluctuation between Japanese yen and the U.S. dollar. Nevertheless, changes in

the exchange rate between the U.S. dollar and the Japanese yen subject our gross profit and operating results to the potential for material fluctuations. Our agreement to purchase wafers from ZMD is denominated in U.S. dollars, as are the purchases we make from our assembly and test suppliers.

Critical Accounting Policies and Estimates

Our critical accounting policies and estimates are as follows:

- revenue recognition;
- estimating sales returns and allowances;
- estimating distributor pricing credits;
- estimating allowance for doubtful accounts;
- estimating reserve for excess and obsolete inventory; and
- income taxes.

We believe that these policies and estimates are important to the portrayal of our financial condition and results and require us to make judgments and estimates about matters that are inherently uncertain. A brief description of these critical accounting policies and estimates is set forth below.

The preparation of financial statements in conformity with accounting principles generally accepted in the United States of America requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosures of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the reporting period. On an on-going basis, we evaluate our estimates, including those related to revenue recognition, sales returns, allowance for distributor pricing credits, bad debts and inventories. We base our estimates on historical facts and various other assumptions that we believe to be reasonable at the time the estimates are made. Actual results could differ from those estimates.

Revenue recognition

Product revenues consist of sales to OEMs, merchant power supply manufacturers and distributors. Shipping terms to international OEMs and merchant power supply manufacturers are delivered at frontier, which is commonly referred to as DAF. As such, title to the product passes to the customer when the shipment reaches the destination country, at which time we recognize the related revenue. Revenue from sales to North American OEMs and merchant power supply manufacturers are recognized upon shipment (FOB-point of origin), as this is when the title is passed to the customer.

Historically, approximately 50% to 60 % of our total sales have been made to distributors pursuant to agreements that allow certain rights of return and protection against subsequent price declines on our products held by these distributors. As a result, we defer the recognition of revenue and the costs of revenues derived from sales to distributors until such distributors resell our products to their customers. We determine the amounts to defer based on the level of actual inventory on hand at our distributors as well as inventory that is in transit to them. The gross profit that is deferred as a result of this policy is reflected as "deferred income on sales to distributors" in the accompanying condensed consolidated balance sheet.

Estimating sales returns and allowances

Net revenue consists of product revenue reduced by estimated sales returns and allowances. To estimate sales returns and allowances, we analyze the following factors: historical returns, current economic trends, levels of inventories of our products held by our customers, and changes in customer demand and acceptance of our products, when we initially establish the reserve and each quarter when we review the adequacy of the reserves. This reserve represents a reserve of the gross margin on estimated future returns and is reflected as a reduction to accounts receivable in the accompanying condensed consolidated balance sheet. Increases to the reserve are recorded as a reduction to net revenue equal to the expected customer credit memo and a corresponding credit is made to cost of sales equal to the estimated cost of the returned product. The net difference, or gross margin, is recorded as an addition to the reserve. Because the reserve for sales returns and allowances is based on our judgments and estimates, particularly as to future customer demand and acceptance of our products, our reserves may not be adequate to cover actual sales returns and other allowances. If our reserves are not adequate, our future net revenues could be adversely affected.

Estimating distributor pricing credits

Frequently, our distributors need a cost lower than the standard distribution price to win business. In these circumstances, the distributor submits a request to us for a lower "sell-in" price on a specific end-customer transaction or a series of transactions. After the distributor ships product to its customer under an approved transaction, the distributor submits a "ship & debit" claim to us to adjust its cost from the standard price to the approved lower price. After verification by us, a credit memo is issued to the distributor to adjust the sell-in price from the standard distribution price to the approved lower price. We maintain a reserve for these credits that appears as a reduction to accounts receivable in our accompanying condensed consolidated balance sheets. Any increase in the reserve results in a corresponding reduction in our net revenues. To establish the adequacy of our reserves, we analyze historical ship and debit amounts and levels of inventory in the distributor channels. If our reserves are not adequate, our net revenues could be adversely affected.

From time to time we will reduce the distribution list price of our products. When this occurs, we give our distributors price protection in the form of credits, on products they hold. The credits are referred to as "price protection". Since we do not recognize revenue until the distributor sells the product to its customers, we generally do not need to provide reserves for price protection. However, in rare instances we must consider price protection in the analysis of reserve requirements, as there may be a timing gap between a price decline and the issuance of price protection credits. If a price protection reserve is required, we will maintain a reserve for these credits that appears as a reduction to accounts receivable in our accompanying condensed consolidated balance sheets. Any increase in the reserve results in a corresponding reduction in our net revenues. We analyze distribution price declines and levels of inventory in the distributor channels on a quarterly basis. If our reserves are not adequate, our net revenues could be adversely affected.

Estimating allowance for doubtful accounts

We maintain an allowance for losses we may incur as a result of our customers' inability to make required payments. Any increase in the allowance results in a corresponding increase in our general and administrative expenses. In establishing this allowance, and then evaluating the adequacy of the allowance for doubtful accounts each quarter, we analyze historical bad debts, customer concentrations, customer credit-worthiness, current economic trends and changes in our customer payment terms. If the financial condition of one or more of our customers deteriorates, resulting in their inability to make payments, or if we otherwise underestimate the losses we incur as a result of our customers' inability to pay us, we could be required to increase our allowance for doubtful accounts which could adversely affect our operating results.

Estimating reserve for excess and obsolete inventory

We identify excess and obsolete products and analyze historical usage, forecasted production based on demand forecasts, current economic trends, and historical write-offs when evaluating the adequacy of the reserve for excess and obsolete inventory . This reserve is reflected as a reduction to inventory in the accompanying condensed consolidated balance sheet, and an increase in cost of revenues. If actual market conditions are less favorable than our assumptions, we may be required to take additional reserves, which could adversely impact our cost of revenues and operating results.

Income taxes

We recognize federal, state and foreign current tax liabilities or assets based on our estimate of taxes payable or refundable in the current fiscal year by tax authorities. We also recognize federal, state and foreign deferred tax liabilities or assets for our estimate of future tax effects attributable to temporary differences and carry forwards and record a valuation allowance to reduce any deferred tax assets by the amount of any tax benefits that, based on available evidence and judgment, are not expected to be realized. As of September 30, 2005, no valuation allowance had been recorded to reduce our deferred tax assets. We believe it is more likely than not that forecasted income, including income that may be generated as a result of certain tax planning strategies, will be sufficient to fully recover our deferred tax assets. In the event that all or part of the net deferred tax assets are determined not to be realizable in the future, a valuation allowance would be recorded in the period such determination is made, which could adversely affect our operating results. In addition, the calculation of tax liabilities involves significant judgment in estimating the impact of uncertainties in the application of complex tax laws. Resolution of these uncertainties in a manner inconsistent with our expectations could have a material impact on our result of operations and financial position.

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Results of Operations

The following table sets forth certain operating data as a percentage of total net revenues for the periods indicated.

	Percentage of Total Net Revenues for Three Months Ended September 30,		Percentage of Total Net Revenues for Nine Months Ended September 30,	
	2005	2004	2005	2004
Net revenues	100.0%	100.0%	100.0%	100.0%
Cost of revenues	50.5	52.2	51.1	52.5
Gross profit	49.5	47.8	48.9	47.5
Operating expenses:				
Research and development	11.2	12.4	11.5	12.0
Sales and marketing	12.1	10.4	12.0	11.1
General and administrative	11.2	7.2	9.2	5.8
Total operating expenses	34.5	30.0	32.7	28.9
Income from operations	15.0	17.8	16.2	18.6
Other income, net	2.5	1.0	2.1	0.7
Income before provision for income taxes	17.5	18.8	18.3	19.3
Provision for income taxes	2.0	1.3	3.8	3.9
Net income	15.5%	17.5%	14.5%	15.4%

Comparison of the Three Months and Nine Months Ended September 30, 2005 and 2004

Net revenues. Net revenues consist of revenues from product sales, which are calculated net of returns and allowances, plus royalties that Matsushita paid to us. Net revenues for the three months ended September 30, 2005 were $36.5 million compared to $32.9 million for the three months ended September 30, 2004, an increase of $3.6 million, or 10.9%. Net revenues for the nine months ended September 30, 2005 were $106.3 million compared to $103.1 million for the comparable period of 2004, an increase of $3.2 million or 3.1%. Our results for the nine months ended September 30, 2005 included an adjustment to our reserve for sales returns and an adjustment to deferred income on sales to distributors, which on a combined basis, increased our net revenue by approximately $2.0 million, and increased our net income by approximately $0.8 million, or $0.03 per diluted share. In the three months ended June 30, 2005 the adjustment to our reserve for sales returns increased net revenues by $0.9 million and increased net income by $0.4 million, or $0.01 per diluted share. In the three months ended March 31, 2005, the change to our method of calculating deferred income on sales to distributors resulted in the recognition of $1.1 million in previously deferred revenue, and an increase in net income of approximately $0.4 million, or $0.01 per diluted share. The impact of these adjustments was not material to any of our prior period financial statements.

Net revenues from product sales were $36.1 million and $32.3 million in the third quarter of 2005 and 2004, respectively. Net revenues from product sales were $104.9 million and $101.3 million in the nine months ended September 30, 2005 and 2004, respectively. The increase in net revenues from product sales for the three and nine months ended September 30, 2005 was driven primarily by increased sales of our products in the computer, industrial and other end markets. Revenues from sales in the computer end market grew 14.8% and 14.4% in the three and nine months ended September 30, 2005, respectively, and sales in the industrial end market grew 59.3% and 27.2% in the three and nine months ended September 30, 2005, respectively, when compared to the same periods a year ago. We showed significant year-over-year growth in product revenues and units shipped despite aggressive price competition.

Revenue mix by product family for the nine months ended September 30, 2005 compared to the twelve months ended December 31, 2004, was as follows:

Product Family	Nine Months Ended Sept 30, 2005	Twelve Months Ended Dec 31, 2004
TinySwitch I and II	56%	54%
TopSwitch FX and GX	28%	28%
TopSwitch I and II	11%	15%
LinkSwitch and DPA-Switch	5%	3%

Approximate revenue mix by end markets served for the nine months ended September 30, 2005 compared to the twelve months ended December 31, 2004, was as follows:

End Market	Nine Months Ended Sept 30, 2005	Twelve Months Ended Dec 31, 2004
Consumer	31%	33%
Communication	29%	31%
Computer	23%	22%
Industrial	10%	8%
Other	7%	6%

Customer demand for our products can change quickly and unexpectedly. Our customers perceive that our products are readily available and typically order only for their short-term needs. Our revenue levels are highly dependent on the amount of new orders that are received for which product can be delivered by us within the same period. Orders that are booked and shipped within the same period are called "turns business." Because of the uncertainty of customer demand, and the short lead-time environment and high turns business, it is difficult to predict future levels of revenues and profitability.

International sales were $34.0 million in the third quarter of 2005 compared to $30.1 million for the same period in 2004, an increase of $3.9 million, or 13.0%. International sales represented 93.0% of net revenues compared to 91.2% in the three months ended September 30, 2005 and 2004, respectively. International sales were $98.7 million for the nine months ended September 30, 2005 compared to $94.6 million for the same period in 2004, an increase of $4.1 million, or 4.0%. International sales represented 92.9% of net revenues compared to 91.8% in the nine months ended September 30, 2005 and 2004, respectively. International sales for the three and nine months ended September 30, 2005 increased due to increased revenue and shipments to our customers primarily in Asia.

Although the power supplies using our products are distributed to end markets worldwide, most of these power supplies are manufactured in Asia. As a result, sales to this region were 77.3% and 73.4% of our sales for the three months ended September 30, 2005 and 2004, respectively, and 77.7% and 76.6% of our sales for the nine months ended September 30, 2005 and 2004, respectively. We expect international sales to continue to account for a large portion of our net revenues.

Net product sales for the third quarter of 2005 were divided 61.3% to distributors and 38.7% to OEMs and power supply merchants, compared to 54.4% to distributors and 45.6% to OEMs and power supply merchants for the third quarter of 2004. For the nine months ended September 30, 2005, net product sales were divided 59.9% to distributors and 40.1% to OEMs and power supply merchants, compared to 55.1% to distributors and 44.9% to OEMs and power supply merchants for the same period in 2004. In the three months ended September 30, 2005, two separate customers, both of who are distributors, accounted for approximately 19.3% and 18.1% of our net revenues, respectively. In the three months ended September 30, 2004, the same two distributors accounted for approximately 15.5% and 17.4% of our net revenues, respectively. No other customers accounted for 10% or more of our net revenues in that period. For the nine months ended September 30, 2005, sales to the same two distributors accounted for approximately 19.4% and 17.3% of our net revenues, respectively, compared to approximately 18.9% and 17.0% of our net revenues, respectively, for the nine months ended September 30, 2004. One OEM customer accounted for approximately 10.7% of our net revenues for the nine months ended September 30, 2004, but accounted for less than 10.0% of our net revenues for the nine months ended September 30, 2005.

Cost of revenues; Gross profit. Gross profit is equal to net revenues less cost of revenues. Our cost of revenues consists primarily of costs associated with the purchase of wafers from our foundries (Matsushita, OKI and ZMD), the assembly and packaging of our products by sub-contractors, internal labor and overhead costs associated with the testing of both wafers and packaged components and testing of packaged components by sub-contractors. Gross profit was $18.1 million, or 49.5% of net revenues, for the three months ended September 30, 2005, compared to $15.8 million, or 47.8% of net revenues, for the three months ended September 30, 2004. Gross profit for the nine months ended September 30, 2005 was $52.0 million, or 48.9% of net revenues, compared to $49.0 million, or 47.5% of net revenues for the same period in 2004. The increase in gross profit percentage for the three and nine months ended September 30, 2005 was driven primarily by our ability to reduce product costs, principally through price reductions from our foundries, improvements to our manufacturing process, and the increased use of overseas subcontractors for the testing of our ICs. We expect our gross margin to remain relatively flat for the rest of 2005, but if pricing pressures increase beyond our expectations, and we are unable to obtain offsetting decreases in our product costs, our gross profit could be lower.

Research and development expenses. Research and development expenses consist primarily of employee-related expenses, expensed engineering material and facility costs associated with the development of new processes and new products. We also expense prototype wafers and mask sets related to new products as research and development costs until new products are released to production. Research and development expenses for the third quarter of 2005 and 2004 were $4.1 million, which represented 11.2% and 12.4% of our net revenues in each period, respectively. Research and development expenses for the nine months ended September 30, 2005 and 2004 were $12.3 million, which represented 11.5% and 12.0% of our net revenues in each period, respectively. We expect in future periods research and development expenses may increase in absolute dollars, but those expenses may fluctuate as a percentage of our net revenues.

Sales and marketing expenses. Sales and marketing expenses consist primarily of employee-related expenses, commissions to sales representatives and facilities expenses, including expenses associated with our regional sales offices and support offices, and field application engineering costs. Sales and marketing expenses were $4.4 million, or 12.1% of net revenues, for the third quarter of 2005, compared to $3.4 million, or 10.4% of net revenues for the same period in 2004. Sales and marketing expenses for the nine months ended September 30, 2005 were $12.7 million compared to $11.5 million for the same period in 2004, which represented 12.0% and 11.1% of our net revenues in each period, respectively. In absolute dollars, sales and marketing expenses for the three and nine months ended September 30, 2005 increased from the same periods in 2004, primarily as a result of expanding our worldwide sales and applications engineering staff. We expect sales and marketing expenses to continue to increase in absolute dollars as we expand our sales and marketing presence worldwide, but these expenses may fluctuate as a percentage of our net revenues.

General and administrative expenses. General and administrative expenses consist primarily of employee-related expenses for administration, finance, human resources and general management, as well as consulting fees, outside services, legal fees and fees for audit and tax services. For the quarters ended September 30, 2005 and 2004, general and administrative expenses were $4.1 million and $2.4 million, respectively, which represented 11.2% and 7.2% of our net revenues, respectively. For the nine months ended September 30, 2005 and 2004, general and administrative expenses were $9.8 million and $6.0 million, respectively, which represented 9.2% and 5.8% of our net revenues, respectively. In absolute dollars, general and administrative expenses for the three and nine month periods in 2005 were higher than in the same periods in 2004, primarily due to a significant increase in legal fees due to the ongoing patent infringement litigation against Fairchild Semiconductor and System General Corporation (as described in Part II Other Information, Item 1 Legal Proceedings), and increased consulting services and audit fees related to compliance with the requirements of the Sarbanes-Oxley Act. We expect general and administrative expenses to increase in absolute dollars generally throughout 2005, primarily as a result of increased patent litigation expenses, but general and administrative expenses may fluctuate as a percentage of our net revenues.

Other income, net. Other income, net, for the third quarter of 2005 was $0.9 million compared to $0.3 million for the same period in 2004. For the nine months ended September 30, 2005, other income, net, was $2.3 million compared to $0.8 million for the same period in 2004. Other income consists primarily of interest income earned on short-term and long-term investments. The increase in other income can be attributed to higher interest rates year-over-year.

Provision for income taxes. Income tax expense for the nine-month periods ended September 30, 2005 and 2004 includes a provision for Federal, state and foreign taxes based on the annual estimated effective tax rate applicable to the Company and its subsidiaries. The difference between the Federal statutory rate of 35% and our effective tax rate used for

the nine-month period ended September 30, 2005 and 2004 is primarily due to the beneficial impact of international sales subject to lower tax rates and research and development tax credits. We adjusted our effective tax rate from 25% to 21% for the nine months ended September 30, 2005 to reflect the estimated annual effective income tax rate for 2005. The change in the estimated effective tax rate for 2005 resulted in an effective tax rate of 12% for the three months ended September 30, 2005. The tax provision for the three and nine month periods ended September 30, 2004 was calculated using an annual effective income tax rate of 26%, which was adjusted for the favorable conclusion of certain tax contingencies in the third quarter of 2004, which resulted in an effective tax rate of approximately 8% and 20% for the three and nine month periods, respectively. The estimated annual effective income tax rate for 2005 may be subject to change in the future.

Liquidity and Capital Resources

As of September 30, 2005, we had approximately $121.8 million in cash, cash equivalents and short-term and long-term investments, a decrease of approximately $12.8 million from December 31, 2004. In addition, under a revolving line of credit with Union Bank of California, we can borrow up to $10.0 million. A portion of the credit line is used to cover advances for commercial letters of credit and standby letters of credit, which we provide to Matsushita, prior to the shipment of wafers by this foundry to us, and also to our workers compensation insurance carrier as part of our insurance program. As of September 30, 2005, there were outstanding letters of credit totaling approximately $2.1 million. The balance of this credit line was unused and available as of September 30, 2005. The line of credit agreement, which expires on June 30, 2006, contains financial covenants requiring that we maintain profitability on a quarterly basis and not pay or declare dividends without the bank's prior consent. As of September 30, 2005, we were in compliance with these financial covenants.

As of September 30, 2005, we had working capital, defined as current assets less current liabilities, of approximately $135.3 million, an increase of approximately $3.0 million from December 31, 2004. Our operating activities generated cash of $22.0 million and $25.1 million in the nine months ended September 30, 2005 and 2004, respectively. Cash generated in the first nine months of 2005 was principally the result of net income in the amount of $15.4 million depreciation and amortization of $4.9 million, and a decrease in inventory of $3.1 million, partially offset by an increase in accounts receivable of $2.6 million and a decrease in accounts payable of $2.2 million. Cash generated in the first nine months of 2004 was principally the result of net income in the amount of $15.9 million plus depreciation and amortization of $5.2 million, income tax benefit associated with our employee stock plan of $2.1 million, and an increase in deferred income of $1.0 million.

Our investing activities in the nine months ended September 30, 2005 included net proceeds of $4.5 million of short-term and long-term investments, the issuance of a $10.0 million promissory note from a supplier (see note 12 of our condensed consolidated financial statements for more information regarding the promissory note from a supplier), and the acquisition of technology for $1.1 million. Our investing activities in the nine months ended September 30, 2004 consisted of net purchases of $18.8 million of short-term and long-term investments. Purchases of property and equipment were $2.3 million as of September 30, 2005, and $4.2 million as of September 30, 2004. Our financing activities for the nine months ended September 30, 2005 included the use of $28.3 million for the repurchase of approximately 1.5 million shares of our common stock, and net proceeds from the issuance of common stock through the exercise of stock options and purchases through our employee stock purchase plan of $7.0 million. In the nine months ended September 30, 2004, our financing activities were primarily receipts from the issuance of common stock through the exercise of stock options and purchases through our employee stock purchase plan of $7.9 million.

On October 20, 2004, we announced that our board of directors had authorized the repurchase of up to $40.0 million of our common stock. The board directed that the repurchases be made pursuant to Rule 10b5-1 of the Exchange Act. From inception of the stock repurchase program in October 2004 through June 30, 2005, we had repurchased 2,033,270 shares for approximately $40.0 million, the total amount authorized by the Company's board of directors. We repurchased 373,270 shares for approximately $8.1 million during the three months ended June 30, 2005, and 1.1 million shares for approximately $20.2 million during the three months ended March 31, 2005. On October 19, 2005 we announced that our board of directors had authorized a second stock repurchase program of up to $25.0 million of our common stock. The board directed that the repurchases be made pursuant to Rule 10b5-1 of the Exchange Act. The repurchases will take place from time to time on the open market.

During the first nine months of 2005, a significant portion of our cash flow was generated by our operations. If our operating results were to deteriorate as a result of decrease in customer demand for our products, or severe pricing pressures from our customers or our competitors, or for other reasons, our ability to generate positive cash flow from

operations may be jeopardized. In that case, we may be forced to use our cash, cash equivalents and short-term investments, or seek financing from third parties to fund our operations. We believe that cash generated from operations, together with existing sources of liquidity, will satisfy our projected working capital and other cash requirements for at least the next 12 months.

Recent Accounting Pronouncements

In December 2004, the FASB issued FASB Staff Position No.109-1 (FAS 109-1), *Application of FASB Statement No.109, Accounting for Income Taxes, to the Tax Deduction on Qualified Production Activities Provided by the American Jobs Creation Act of 2004* (the AJCA). The AJCA introduces a special 9% tax deduction on qualified production activities. FAS 109-1 clarifies that this tax deduction should be accounted for as a special tax deduction in accordance with Statement 109. We are currently evaluating the impact of FAS 109-1, however we do not believe it will have a material impact on our financial statements.

In December 2004, the Financial Accounting Standards Board (FASB) issued Statement of Financial Accounting Standards (SFAS) No. 123 (revised 2004) *Share-Based Payment* (SFAS 123R), which replaces SFAS No. 123 *Accounting for Stock-Based Compensation* (SFAS 123) and supersedes APB Opinion No. 25 *Accounting for Stock Issued to Employees* . The pro forma disclosures previously permitted under SFAS 123 no longer will be an alternative to financial statement recognition. Under SFAS 123(R), beginning January 1, 2006, we must determine the appropriate fair value model to be used for valuing share-based payments, the amortization method for compensation cost and the transition method to be used at the date of adoption. The transition methods include a modified-prospective and a modified-retroactive adoption options. Under the modified-retroactive option, prior periods may be restated either as of the beginning of the year of adoption or for all periods presented. The modified-prospective method requires that compensation expense be recorded for all unvested stock options and restricted stock at the beginning of the first quarter of adoption of SFAS 123(R), while the modified-retroactive methods would record compensation expense for all unvested stock options and restricted stock beginning with the first period restated. We are currently evaluating the requirements of SFAS 123(R), and expect that the adoption of SFAS 123(R) will have a material impact on our consolidated results of operations and earnings per share. We have decided to use the Black-Scholes closed-form model valuation technique to value our share options, and it has not been determined whether the adoption of this valuation method will result in amounts that are similar to the current pro forma disclosures under SFAS 123.

In March 2005, the SEC issued Staff Accounting Bulletin 107 (SAB 107), *Share-Based Payment* , which expresses views of the SEC staff regarding the application of SFAS No. 123(R). Among other things, SAB 107 provides interpretive guidance related to the interaction between SFAS No. 123(R) and certain SEC rules and regulations, as well as the SEC staff's views regarding the valuation of share-based payment arrangements for public companies.

In March 2005, the FASB issued FSP No. 46(R)-5, *Implicit Variable Interests under FASB Interpretation No. 46 (revised December 2003), Consolidation of Variable Interest Entities* (FSP 46(R)-5), which provides guidance for a reporting enterprise on whether it holds an implicit variable interest in a variable interest entity (VIE) or potential VIE when specific conditions exist. FSP 46(R)-5 became applicable for us in the quarter ended June 30, 2005. FSP 46(R) had no impact on our consolidated results of operation and financial condition as of September 30, 2005.

In March 2005, the FASB issued FIN 47, *Accounting for Conditional Asset Retirement Obligations, an interpretation of FASB Statement No. 143* (FIN 47), which requires an entity to recognize a liability for the fair value of a conditional asset retirement obligation when incurred if the liability's fair value can be reasonably estimated. FIN 47 is effective for fiscal years ending after December 15, 2005. We are currently evaluating the effect that the adoption of FIN 47 will have on our consolidated results of operations and financial condition, however we do not expect it to have a material impact.

In May 2005, the FASB issued SFAS No. 154, *Accounting Changes and Error Corrections* (SFAS 154) that replaces Accounting Principles Board Opinions No. 20 *Accounting Changes* and SFAS No. 3, *Reporting Accounting Changes in Interim Financial Statements—An Amendment of APB Opinion No. 28* . SFAS 154 provides guidance on the accounting for and reporting of accounting changes and error corrections. It establishes retrospective application, or the latest practicable date, as the required method for reporting a change in accounting principle and the reporting of a correction of an error. SFAS 154 is effective for accounting changes and corrections of errors made in fiscal years beginning after December 15, 2005 and is required to be adopted by us in the first quarter of fiscal 2006. We are currently evaluating the effect that the adoption of SFAS 154 will have on our consolidated results of operations and financial condition but we do not expect it to have a material impact.

Factors That May Affect Future Results of Operations

In addition to the other information in this report, the following factors should be considered carefully in evaluating our business before purchasing shares of our stock.

Our quarterly operating results are volatile and difficult to predict. If we fail to meet the expectations of public market analysts or investors, the market price of our common stock may decrease significantly . Our net revenues and operating results have varied significantly in the past, are difficult to forecast, are subject to numerous factors both within and outside of our control, and may fluctuate significantly in the future. As a result, our quarterly operating results could fall below the expectations of public market analysts or investors. If that occurs, the price of our stock may decline.

Some of the factors that could affect our operating results include the following:

- the volume and timing of orders received from customers;
- competitive pressures on selling prices;
- the demand for our products declining in the major end markets we serve;
- continued impact of recently enacted changes in securities laws and regulations, including the Sarbanes-Oxley Act of 2002;
- the inability to adequately protect or enforce our intellectual property rights;
- expenses we are required to incur in connection with our litigation against Fairchild Semiconductor and System General Corporation;
- changes to generally accepted accounting principles (GAAP) which will require recording compensation expense for employee stock options and employee stock purchase plans;
- the volume and timing of orders placed by us with our wafer foundries and assembly subcontractors;
- fluctuations in exchange rates, particularly the exchange rates between the U.S. dollar and the Japanese yen;
- the licensing of our intellectual property to one of our wafer foundries;
- the lengthy timing of our sales cycle;
- undetected defects and failures in meeting the exact specifications required by our products;
- our international sales activities account for a substantial portion of our net revenues which subjects us to substantial risks;
- our ability to develop and bring to market new products and technologies on a timely basis;
- the ability of our products to penetrate additional markets;
- attraction and retention of qualified personnel in a competitive market;
- changes in environmental laws and regulations;
- the adoption of anti-takeover measures;
- the volatility of the future trading price of our common stock, and
- earthquakes, terrorists acts or other disasters.

We do not have long-term contracts with any of our customers and if they fail to place, or if they cancel or reschedule orders for our products, our operating results and business may suffer. Our business is characterized by short-term customer orders and shipment schedules. Our customer base is highly concentrated, and a relatively small number of distributors, OEMs and merchant power supply manufacturers account for a significant portion of our revenues. The ordering patterns of some of our existing large customers have been unpredictable in the past and we expect that customer-ordering patterns will continue to be unpredictable in the future. Not only does the volume of units ordered by particular customers vary substantially from period to period, but also purchase orders received from particular customers

often vary substantially from early oral estimates provided by those customers for planning purposes. In addition, customer orders can be canceled or rescheduled without significant penalty to the customer. In the past we have experienced customer cancellations of substantial orders for reasons beyond our control, and significant cancellations could occur again at any time.

Intense competition in the high-voltage power supply industry may lead to a decrease in the average selling price and reduced sales volume of our products, which may harm our business . The high-voltage power supply industry is intensely competitive and characterized by significant price erosion. Our products face competition from alternative technologies, such as, traditional linear transformers, discrete switcher power supplies, and other integrated and hybrid solutions. If the price of competing solutions decreases significantly, the cost effectiveness of our products will be adversely affected. If power requirements for applications in which our products are currently utilized go outside the cost effective range of our products, some of these alternative technologies can be used more cost effectively. We cannot assure that our products will continue to compete favorably or that we will be successful in the face of increasing competition from new products and enhancements introduced by existing competitors or new companies entering this market. We believe our failure to compete successfully in the high-voltage power supply business, including our ability to introduce new products with higher average selling prices, would materially harm our operating results.

If demand for our products declines in the major end markets that we serve, our net revenues will decrease . Applications of our products in the consumer, communications and computer end markets, such as cellular phone chargers, stand-by power supplies for PCs, power supplies for TV set top boxes and power supplies for home appliances have and will continue to account for a large percentage of our net revenues. We expect that a significant level of our net revenues and operating results will continue to be dependent upon these applications in the near term. The demand for these products has been highly cyclical and has been subject to significant economic downturns at various times. Announcements of economic slowdown by major companies in any of the end markets we serve, could indirectly through our customers, cause a slowdown in demand for some of our ICs. When our customers are not successful in maintaining high levels of demand for their products, their demand for our ICs decreases, which adversely affects our operating results. Any significant downturn in demand in these markets would cause our net revenues to decline and could cause the price of our stock to fall.

Recently enacted changes in securities laws and regulations will continue to increase our costs . Complying with the requirements of the Sarbanes-Oxley Act of 2002, and Nasdaq's revised conditions for continued listing on Nasdaq has increased, and will continue to increase our legal and financial compliance costs, and make some activities more difficult, time consuming and/or costly. These new rules and regulations also may make it more expensive for us to obtain director and officer liability insurance, and we may be required to accept reduced coverage or incur substantially higher costs to obtain coverage. These new rules and regulations could also make it more difficult for us to attract and retain qualified members of our board of directors, particularly qualified members to serve on our audit committee, and qualified executive officers.

Additionally, our efforts to comply with Section 404 of the Sarbanes-Oxley Act and the related regulations regarding our required assessment of our internal controls over financial reporting and our external auditors' audit of the assessment of our internal controls continues to require the commitment of significant financial and managerial resources. Although we believe that the ongoing review of our internal controls over financial reporting will enable us to provide an assessment of our internal controls and our external auditors to provide their audit opinion, we can give no assurance that such assessment will continue to be successfully completed.

Moreover, because these laws, regulations and standards promulgated by the Sarbanes-Oxley Act are subject to varying interpretations, their application in practice may evolve over time as new guidance becomes available. This evolution may result in continuing uncertainty regarding compliance matters and additional costs necessitated by ongoing revisions to our disclosure and governance practices.

If we are unable to adequately protect or enforce our intellectual property rights, we could lose market share, incur costly litigation expenses, suffer incremental price erosion or lose valuable assets, any of which could harm our operations and negatively impact our profitability . Our success depends upon our ability to protect our intellectual property, including patents, trade secrets, copyrights, and know-how, and to continue our technological innovation. We cannot assure that the steps we have taken to protect our intellectual property will be adequate to prevent misappropriation or that others will not develop competitive technologies or products. From time to time we have received, and we may receive in the future, communications alleging possible infringement of patents or other intellectual property rights of others. Litigation, which could result in substantial cost to us, may be necessary to enforce our patents or other intellectual

property rights or to defend us against claimed infringement of the rights of others. The failure to obtain necessary licenses or other rights or litigation arising out of infringement claims could cause us to lose market share and harm our business.

There can be no assurance that we will prevail in our litigation with either System General or Fairchild. This litigation, whether or not determined in our favor or settled by us, will be costly and will divert the efforts and attention of our management and technical personnel from normal business operations, which could have a material adverse effect on our business, financial condition and operating results. Adverse determinations in litigation could result in the loss of our proprietary rights, subject us to significant liabilities, require us to seek licenses from third parties or prevent us from licensing our technology, any of which could have a material adverse effect on our business, financial condition and operating results.

Moreover, the laws of some foreign countries in which our technology is or may in the future be licensed may not protect our intellectual property rights to the same extent as the laws of the United States, thus increasing the possibility of infringement of our intellectual property.

Changes to GAAP that will require recording compensation expense for employee stock options and employee stock purchase plans. The FASB recently enacted SFAS 123(R), which will require us to adopt a different method of determining the compensation expense of our employee stock options and employee stock purchase plan. We have elected to adopt the Black-Scholes closed-form model valuation technique to value our stock options. We believe this valuation technique, which we will begin applying in the quarter ended March 31, 2006 will have a significant adverse effect on our reported financial conditions and may impact the way we conduct our business.

We depend on third-party suppliers to provide us with wafers for our products and if they fail to provide us sufficient wafers, our business may suffer. We have supply arrangements for the production of wafers with Matsushita, which expires in June 2010, with OKI, which expires in April 2008, and with ZMD, which expires in December 2009. Although certain aspects of our relationships with Matsushita, OKI and ZMD are contractual, many important aspects of these relationships depend on their continued cooperation. We cannot assure that we will continue to work successfully with Matsushita, OKI or ZMD in the future, that the wafer foundries' capacity will meet our needs, or that any of them will not seek an early termination of our wafer supply agreements. Any serious disruption in the supply of wafers from OKI, Matsushita or ZMD could harm our business. We estimate that it would take 9 to 18 months from the time we identified an alternate manufacturing source before that source could produce wafers with acceptable manufacturing yields in sufficient quantities to meet our needs.

Although we provide our foundries with rolling forecasts of our production requirements, their ability to provide wafers to us is ultimately limited by the available capacity of the wafer foundry in which they manufacture wafers for us. Any reduction in wafer foundry capacity available to us could require us to pay amounts in excess of contracted or anticipated amounts for wafer deliveries or require us to make other concessions in order to acquire the wafer supply necessary to meet our customers' requirements. Any of these concessions could harm our business.

If our third-party suppliers and independent subcontractors do not produce our wafers and assemble our finished products at acceptable yields, our net revenues may decline. We depend on independent foundries to produce wafers, and independent subcontractors to assemble and test finished products, at acceptable yields and to deliver them to us in a timely manner. The failure of the foundries to supply us wafers at acceptable yields could prevent us from selling our products to our customers and would likely cause a decline in our net revenues. In addition, our IC assembly process requires our manufacturers to use a high-voltage molding compound available from only one vendor, which is difficult to process. This compound and its required processes, together with the other non-standard materials and processes needed to assemble our products, require a more exacting level of process control than normally required for standard packages. Unavailability of the sole source compound or problems with the assembly process can materially adversely affect yields, timely delivery and cost to manufacture. We cannot assure that acceptable yields will be maintainable in the future.

Fluctuations in exchange rates, particularly the exchange rates between the U.S. dollar and the Japanese yen may impact our gross margin. The contract prices to purchase wafers from Matsushita and OKI are denominated in Japanese yen. The agreements with both vendors allow for mutual sharing of the impact of the exchange rate fluctuation between Japanese yen and the U.S. dollar. Nevertheless, changes in the exchange rate between the U.S. dollar and the Japanese yen subject our gross profit and operating results to the potential for material fluctuations.

Matsushita has licenses to our technology, which it may use to our detriment. Pursuant to a Technology Agreement with Matsushita, which expired in June 2005, Matsushita has the perpetual right to manufacture and sell products that incorporate our technology, as of June 2005, to Japanese companies worldwide and to subsidiaries of Japanese companies located in Asia. Matsushita does not have rights to any technology that we develop beyond June 2005. As per the expired Technology Agreement, we will continue to receive royalties on Matsushita's sales through June 2009 at a reduced rate. However, these royalties are substantially lower than the gross profit we receive on direct sales, and we cannot assure that Matsushita will not use the technology rights to continue to develop and market competing products.

Because the sales cycle for our products can be lengthy, we may incur substantial expenses before we generate significant revenues, if any. Our products are generally incorporated into a customer's products at the design stage. However, customer decisions to use our products, commonly referred to as design wins, which can often require us to expend significant research and development and sales and marketing resources without any assurance of success, often precede volume sales, if any, by a year or more. The value of any design win will largely depend upon the commercial success of the customer's product. We cannot assure that we will continue to achieve design wins or that any design win will result in future revenues. If a customer decides at the design stage not to incorporate our products into its product, we may not have another opportunity for a design win with respect to that product for many months or years.

Our products must meet exacting specifications, and undetected defects and failures may occur which may cause customers to return or stop buying our products. Our customers generally establish demanding specifications for quality, performance and reliability that our products must meet. ICs as complex as those we sell often encounter development delays and may contain undetected defects or failures when first introduced or after commencement of commercial shipments. We have from time to time in the past experienced product quality, performance or reliability problems. If defects and failures occur in our products, we could experience lost revenue, increased costs, including warranty expense and costs associated with customer support and customer expenses, delays in or cancellations or rescheduling of orders or shipments and product returns or discounts, any of which would harm our operating results.

Our international sales activities account for a substantial portion of our net revenues, which subjects us to substantial risks. Sales to customers outside of the United States account for, and have accounted for a large portion of our net revenues, including approximately 93% and 91% of our net revenues for the nine months ended September 30, 2005 and 2004, respectively. If our international sales declined and we were unable to increase domestic sales, our revenues would decline and our operating results would be harmed. International sales involve a number of risks to us, including:

- potential insolvency of international distributors and representatives;
- reduced protection for intellectual property rights in some countries;
- the impact of recessionary environments in economies outside the United States;
- tariffs and other trade barriers and restrictions;
- the burdens of complying with a variety of foreign and applicable U.S. Federal and state laws; and
- foreign currency exchange risk.

Our failure to adequately address these risks could reduce our international sales, which would materially adversely affect our operating results. Furthermore, because substantially all of our foreign sales are denominated in U.S. dollars, increases in the value of the dollar increase the price in local currencies of our products in foreign markets and make our products relatively more expensive and less price competitive than competitors' products that are priced in local currencies.

If our efforts to enhance existing products and introduce new products are not successful, we may not be able to generate demand for our products . Our success depends in significant part upon our ability to develop new ICs for high-voltage power conversion for existing and new markets, to introduce these products in a timely manner and to have these products selected for design into products of leading manufacturers. New product introduction schedules are subject to the risks and uncertainties that typically accompany development and delivery of complex technologies to the market place, including product development delays and defects. If we fail to develop and sell new products in a timely manner, our net revenues could decline.

In addition, we cannot be sure that we will be able to adjust to changing market demands as quickly and cost-effectively as necessary to compete successfully. Furthermore, we cannot assure that we will be able to introduce new products in a timely and cost-effective manner or in sufficient quantities to meet customer demand or that these products will achieve market acceptance. Our failure, or our customers' failure to develop and introduce new products successfully and in a timely manner would harm our business and may cause the price of our common stock to fall. In addition, customers may defer or return orders for existing products in response to the introduction of new products. Although we maintain reserves for potential customer returns, we cannot assure that these reserves will be adequate.

If our products do not penetrate additional markets, our business will not grow as we expect. We believe that our future success depends in part upon our ability to penetrate additional markets for our products. We cannot assure that we will be able to overcome the marketing or technological challenges necessary to do so. To the extent that a competitor penetrates additional markets before we do, or takes market share from us in our existing markets, our net revenues and financial condition could be materially adversely affected.

We must attract and retain qualified personnel to be successful and competition for qualified personnel is intense in our market. Our success depends to a significant extent upon the continued service of our executive officers and other key management and technical personnel, and on our ability to continue to attract, retain and motivate qualified personnel, such as experienced analog design engineers and systems applications engineers. The competition for these employees is intense, particularly in Silicon Valley. The loss of the services of one or more of our engineers, executive officers or other key personnel could harm our business. In addition, if one or more of these individuals leaves our employ, and we are unable to quickly and efficiently replace those individuals with qualified personnel who can smoothly transition into their new roles, our business may suffer. We do not have long-term employment contracts with, and we do not have in place key person life insurance policies on, any of our employees.

Changes in environmental laws and regulations may potentially increase our costs related to obsolete products in our existing inventory . Changing environmental regulations and the timetable to implement them are continuing to modify our customers demand for our products. As a result there could be an increase in our inventory obsolescence costs for products manufactured prior to our customer's adoption of new regulations. Currently we have limited visibility into our customers' strategies to implement these changing environmental regulations into their business. The inability to accurately determine our customer's strategies could increase our inventory costs related to obsolescence.

We have adopted anti-takeover measures, which may make it more difficult for a third party to acquire us. Our board of directors has the authority to issue up to 3,000,000 shares of preferred stock and to determine the price, rights, preferences and privileges of those shares without any further vote or action by the stockholders. The rights of the holders of common stock will be subject to, and may be adversely affected by, the rights of the holders of any preferred stock that may be issued in the future. The issuance of shares of preferred stock, while potentially providing flexibility in connection with possible acquisitions and for other corporate purposes, could have the effect of making it more difficult for a third party to acquire a majority of our outstanding voting stock. We have no present intention to issue shares of preferred stock.

In addition, our board of directors adopted a Preferred Stock Purchase Rights Plan intended to guard against hostile takeover tactics. The existence of this plan could have the effect of making it more difficult for a third party to acquire a majority of our outstanding voting stock.

The future trading price of our common stock could be subject to wide fluctuations in response to a variety of factors. The price of our common stock has been, and is likely to be, volatile. Factors including future announcements concerning us, our customers or our competitors, quarterly variations in operating results, announcements of technological innovations, the introduction of new products or changes in our product pricing policies or those of our competitors, proprietary rights or other litigation, changes in earnings estimates by analysts and other factors could cause the market price of our common stock to fluctuate substantially. In addition, stock prices for many technology companies fluctuate widely for reasons, which may be unrelated to operating results. These fluctuations, as well as general economic, market and political conditions may harm the market price of our common stock.

In the event of an earthquake, terrorist act or other disaster, our operations may be interrupted and our business would be harmed. Our principal executive offices and operating facilities situated near San Francisco, California, and most of our major suppliers (wafer foundries and assembly houses), are located in areas that have been subject to severe earthquakes. In the event of an earthquake, we and/or most of our major suppliers may be temporarily unable to continue operations and may suffer significant property damage. Any such interruption in our ability or that of our major suppliers to continue operations at our facilities could delay the development and shipment of our products.

Like other U.S. companies, our business and operating results are subject to uncertainties arising out of economic consequences of current and potential military actions or terrorist activities and associated political instability, and the impact of heightened security concerns on domestic and international travel and commerce. Such uncertainties could also lead to delays or cancellations of customer orders, a general decrease in corporate spending or our inability to effectively market and sell our products. Any of these results could substantially harm our business and results of operations, causing a decrease in our revenues.

ITEM 3. QUANTITATIVE AND QUALITATIVE DISCLOSURE ABOUT MARKET RISKS.

There has not been a material change in our exposure to interest rate and foreign currency risks from that described in our 2004 Annual Report on Form 10-K.

Interest Rate Risk. Our exposure to market risk for changes in interest rates relates primarily to our investment portfolio. We do not use derivative financial instruments in our investment portfolio to manage our interest rate risk, foreign currency risk, or for any other purpose. We invest in high-credit quality issuers and, by policy, limit the amount of credit exposure to any one issuer. As stated in our policy, we ensure the safety and preservation of our invested principal funds by limiting default risk, market risk and reinvestment risk. We mitigate default risk by investing in safe and high-credit quality securities and by constantly positioning our portfolio to respond appropriately to a significant reduction in a credit rating of any investment issuer, guarantor or depository. The portfolio includes only marketable securities with active secondary or resale markets to ensure portfolio liquidity.

The table below presents carrying value and related weighted average interest rates for our investment portfolio at September 30, 2005.

(in thousands, except average interest rates)

	Carrying Value	Average Interest Rate
Investment Securities Classified as Cash Equivalents:		
Taxable securities	$ 81,011	3.81%
Investment Securities Classified as Short-term Investments:		
U.S. corporate securities	1,939	2.23%
U.S. government securities	12,799	3.21%
Total	14,738	3.08%
Investment Securities Classified as Long-term Investments:		
U.S. government securities	6,958	2.82%
Total investment securities	$102,707	3.64%

Foreign Currency Exchange Risk. We transact business in various foreign countries. Our primary foreign currency cash flows are in Asia and Western Europe. Currently, we do not employ a foreign currency hedge program utilizing foreign currency forward exchange contracts; however, the contract prices to purchase wafers from Matsushita and OKI are denominated in Japanese yen and both agreements allow for mutual sharing of the impact of the exchange rate fluctuation between Japanese yen and the U.S. dollar. Nevertheless, changes in the exchange rate between the U.S. dollar and the Japanese yen subject our gross profit and operating results to the potential for material fluctuations. We maintain a Japanese yen account with a U. S. bank for payments to our wafer suppliers in Japan.

ITEM 4. CONTROLS AND PROCEDURES.

(a) Under the supervision and with the participation of our management, including our chief executive officer and chief financial officer, we evaluated the effectiveness of the design and operation of our disclosure controls and procedures, as such term is defined under Rule 13a-15 (e) promulgated under the Securities Exchange Act of 1934, as amended, as of the end of the period covered by this report. Based on this evaluation, our chief executive officer and chief financial officer concluded that our disclosure controls and procedures were effective as of that date.

(b) There has been no change in our internal control over financial reporting during the quarter ended September 30, 2005, that has materially affected, or is reasonably likely to materially affect, our internal control over financial reporting.

PART II. OTHER INFORMATION

ITEM 1. LEGAL PROCEEDINGS

On June 28, 2004, the Company filed a complaint for patent infringement in the U.S. District Court, Northern District of California, against System General Corporation, a Taiwanese company and its U.S. subsidiary. The Company's complaint alleges that certain integrated circuits produced by System General Corporation infringed and continue to infringe certain of the Company's patents. The Company seeks, among other things, an order enjoining System General Corporation from infringing the Company's patents and an award for damages resulting from the alleged infringement.

On May 9, 2005, the Company filed a complaint with the U.S. International Trade Commission (ITC) under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. section 1337, naming System General Corporation of Taiwan as the respondent. The Company filed a supplement to the complaint on May 24, 2005. The Company alleges infringement by System General of the same patents raised in the action in the Northern District of California. The ITC instituted an investigation on June 8, 2005 in response to the Company's complaint. By its complaint, the Company seeks an order from the ITC excluding System General's PWM chips and the products containing them, such as LCD monitors, from importation into the United States. The ITC hearing is scheduled to begin on January 18, 2006, based on the hearing, the judge will make an initial determination of weather System General is infringing the Company's patents. On June 10, 2005, in response to the initiation of the ITC investigation, the District Court stayed all proceedings.

On October 20, 2004, the Company filed a complaint for patent infringement in the U.S. District Court for the District of Delaware, against Fairchild Semiconductor International, Inc., a Delaware corporation, and Fairchild Semiconductor Corporation, a Delaware corporation (collectively, Fairchild). The Company's complaint alleges that Fairchild produces certain integrated circuits, which infringed and continue to infringe certain of the Company's patents. The Company seeks, among other things, an order enjoining Fairchild from infringing the Company's patents and an award for damages resulting from the alleged infringement.

There can be no assurance that the Company will prevail in its litigation with either System General or Fairchild. This litigation, whether or not determined in the Company's favor or settled by the Company, will be costly and will divert the efforts and attention of the Company's management and technical personnel from normal business operations, which could have a material adverse effect on the Company's business, financial condition and operating results. Adverse determinations in litigation could result in the loss of the Company's proprietary rights, subject the Company to significant liabilities, require the Company to seek licenses from third parties or prevent the Company from licensing its technology, any of which could have a material adverse effect on the Company's business, financial condition and operating results.

ITEM 2. UNREGISTERED SALES OF EQUITY SECURITIES AND USE OF PROCEEDS

On October 20, 2004, the Company announced that its board of directors had authorized the repurchase of up to $40.0 million of the Company's common stock. The board directed that the repurchases be made pursuant to Rule 10b5-1 of the Exchange Act. From inception of the stock repurchase program in October 2004 through June 30, 2005, the Company repurchased 2,033,270 shares for approximately $40.0 million, the total amount authorized by the Company's board of directors. The Company repurchased 373,270 shares for approximately $8.1 million during the three months ended June 30, 2005, and 1.1 million shares for approximately $20.2 million during the three months ended March 31, 2005. On October 19, 2005 the Company announced that its board of directors had authorized a second stock repurchase program of up to $25.0 million of the Company's common stock. The board directed that the repurchases be made pursuant to Rule 10b5-1 of the Exchange Act. The repurchases will take place from time to time on the open market.

ITEM 3. DEFAULTS UPON SENIOR SECURITIES

None.

ITEM 4. SUBMISSION OF MATTERS TO VOTE OF SECURITY HOLDERS

None.

ITEM 5. OTHER INFORMATION

None.

ITEM 6. EXHIBITS

Exhibit Number	Description
31.1	Certification of Chief Executive Officer pursuant to Section 302(a) of the Sarbanes-Oxley Act of 2002
31.2	Certification of Chief Financial Officer pursuant to Section 302(a) of the Sarbanes-Oxley Act of 2002
32.1	Certification of Chief Executive Officer pursuant to Section 906 of the Sarbanes-Oxley Act of 2002
32.2	Certification of Chief Financial Officer pursuant to Section 906 of the Sarbanes-Oxley Act of 2002

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

POWER INTEGRATIONS, INC.

Date: November 7, 2005

By: /s/ JOHN M. COBB

John M. Cobb
Chief Financial Officer

Exhibit 31.1

CERTIFICATIONS

I, Balu Balakrishnan, Chief Executive Officer of the registrant, certify that:

1. I have reviewed this quarterly report on Form 10-Q of Power Integrations, Inc.;

2. Based on my knowledge, this report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this report;

3. Based on my knowledge, the financial statements, and other financial information included in this report, fairly present in all material respects the financial condition, results of operations and cash flows of the registrant as of, and for, the periods presented in this report;

4. The registrant's other certifying officer and I are responsible for establishing and maintaining disclosure controls and procedures (as defined in Exchange Act Rules 13a-15(e) and 15d-15(e)) and internal control over financial reporting (as defined in Exchange Act Rules 13a-15(f) and 15d-15(f)) for the registrant and have:

(a) Designed such disclosure controls and procedures, or caused such disclosure controls and procedures to be designed under our supervision, to ensure that material information relating to the registrant, including its consolidated subsidiaries, is made known to us by others within those entities, particularly during the period in which this report is being prepared;

(b) Designed such internal control over financial reporting, or caused such internal control over financial reporting to be designed under our supervision, to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with generally accepted accounting principles;

(c) Evaluated the effectiveness of the registrant's disclosure controls and procedures and presented in this report our conclusions about the effectiveness of the disclosure controls and procedures, as of the end of the period covered by this report based on such evaluation; and

(d) Disclosed in this report any change in the registrant's internal control over financial reporting that occurred during the registrant's most recent fiscal quarter that has materially affected, or is reasonably likely to materially affect, the registrant's internal control over financial reporting; and

5. The registrant's other certifying officer and I have disclosed, based on our most recent evaluation of internal control over financial reporting, to the registrant's auditors and the audit committee of the registrant's board of directors (or persons performing the equivalent functions):

(a) All significant deficiencies and material weaknesses in the design or operation of internal control over financial reporting which are reasonably likely to adversely affect the registrant's ability to record, process, summarize and report financial information; and

(b) Any fraud, whether or not material, that involves management or other employees who have a significant role in the registrant's internal control over financial reporting.

Dated: November 7, 2005

By: /s/ B ALU B ALAKRISHNAN

Balu Balakrishnan
Chief Executive Officer

Exhibit 31.2

CERTIFICATIONS

I, John M. Cobb, Chief Financial Officer of the registrant, certify that:

1. I have reviewed this quarterly report on Form 10-Q of Power Integrations, Inc.;

2. Based on my knowledge, this report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this report;

3. Based on my knowledge, the financial statements, and other financial information included in this report, fairly present in all material

respects the financial condition, results of operations and cash flows of the registrant as of, and for, the periods presented in this report;

4. The registrant's other certifying officer and I are responsible for establishing and maintaining disclosure controls and procedures (as defined in Exchange Act Rules 13a-15(e) and 15d-15(e)) and internal control over financial reporting (as defined in Exchange Act Rules 13a-15(f) and 15d-15(f)) for the registrant and have:

(a) Designed such disclosure controls and procedures, or caused such disclosure controls and procedures to be designed under our supervision, to ensure that material information relating to the registrant, including its consolidated subsidiaries, is made known to us by others within those entities, particularly during the period in which this report is being prepared;

(b) Designed such internal control over financial reporting, or caused such internal control over financial reporting to be designed under our supervision, to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with generally accepted accounting principles;

(c) Evaluated the effectiveness of the registrant's disclosure controls and procedures and presented in this report our conclusions about the effectiveness of the disclosure controls and procedures, as of the end of the period covered by this report based on such evaluation; and

(d) Disclosed in this report any change in the registrant's internal control over financial reporting that occurred during the registrant's most recent fiscal quarter that has materially affected, or is reasonably likely to materially affect, the registrant's internal control over financial reporting; and

5. The registrant's other certifying officer and I have disclosed, based on our most recent evaluation of internal control over financial reporting, to the registrant's auditors and the audit committee of the registrant's board of directors (or persons performing the equivalent functions):

(a) All significant deficiencies and material weaknesses in the design or operation of internal control over financial reporting which are reasonably likely to adversely affect the registrant's ability to record, process, summarize and report financial information; and

(b) Any fraud, whether or not material, that involves management or other employees who have a significant role in the registrant's internal control over financial reporting.

Dated: November 7, 2005

By: /s/ JOHN M. COBB

John M. Cobb
Chief Financial Officer

Exhibit 32.1

CERTIFICATION OF CHIEF EXECUTIVE OFFICER

CERTIFICATION PURSUANT TO 18 U.S.C. SECTION 1350, AS ADOPTED PURSUANT TO SECTION 906 OF THE SARBANES-OXLEY ACT OF 2002

In connection with the Quarterly Report of Power Integrations, Inc. (the "Company") on Form 10-Q for the quarter ended September 30, 2005, as filed with the Securities and Exchange Commission on the date hereof (the "Report"), I, Balu Balakrishnan, Chief Executive Officer of the Company, certify, pursuant to 18 U.S.C. Section 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002 ("Section 906"), that:

(1) the Report fully complies with the requirements of section 13(a) of the Securities Exchange Act of 1934 (15 U.S.C. 78m); and

(2) the information contained in the Report fairly presents, in all material respects, the financial condition and results of operations of the Company.

Dated: November 7, 2005

By: /S/ B ALU B ALAKRISHNAN

Balu Balakrishnan
Chief Executive Officer

A signed original of this written statement required by Section 906, or other document authenticating, acknowledging, or otherwise adopting the signature that appears in typed form within the electronic version of this written statement required by Section 906, has been provided to the Company and will be retained by the Company and furnished to the Securities and Exchange Commission or its staff upon request.

Exhibit 32.2

CERTIFICATION OF CHIEF FINANCIAL OFFICER

CERTIFICATION PURSUANT TO 18 U.S.C. SECTION 1350, AS ADOPTED PURSUANT TO SECTION 906 OF THE SARBANES-OXLEY ACT OF 2002

In connection with the Quarterly Report of Power Integrations, Inc. (the "Company") on Form 10-Q for the quarter ended September 30, 2005, as filed with the Securities and Exchange Commission on the date hereof (the "Report"), I, John M. Cobb, Chief Financial Officer of the Company, certify, pursuant to 18 U.S.C. Section 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002 ("Section 906"), that:

(1) the Report fully complies with the requirements of section 13(a) of the Securities Exchange Act of 1934 (15 U.S.C. 78m); and

(2) the information contained in the Report fairly presents, in all material respects, the financial condition and results of operations of the Company.

Dated: November 7, 2005

By: /s/ JOHN M. COBB

John M. Cobb
Chief Financial Officer

A signed original of this written statement required by Section 906, or other document authenticating, acknowledging, or otherwise adopting the signature that appears in typed form within the electronic version of this written statement required by Section 906, has been provided to the Company and will be retained by the Company and furnished to the Securities and Exchange Commission or its staff upon request.

End of Filing

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TECHNICAL DIGEST

international

ELECTRON DEVICES meeting

19

WASHINGTON, D.C.

December 3–4–5

Late News!
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HIGH VOLTAGE THIN LAYER DEVICES (RESURF DEVICES)

J.A. Appels and H.M.J. Vaes

Philips Research Laboratories
Eindhoven - The Netherlands

ABSTRACT

The application of a somewhat unusual diode structure opens the possibility to make novel kinds of high voltage devices even with very thin epitaxial or implanted layers. In the new structures crucial changes in the electric field distribution take place at or at least near the surface. The acronym RESURF (REduced SURface Field) was chosen.

BASIC STRUCTURE

The basic structure consists of a high-ohmic P^- substrate with an epitaxial N^- layer on it, which is laterally bounded by a P^+ diffusion[1]. The diode thus formed consists of two parts: one horizontal P^-N junction and a vertical P^+N junction. Considering these parts as one-dimensional junctions, the vertical one has the lower breakdown voltage, which is determined by the doping concentration of the epitaxial layer (e.g. 370 V for $N_{epi} = 6.10^{14}$). The breakdown voltage of the horizontal junction is considerably higher due to the high-ohmic substrate (1150 V for the example of fig. 1).
For thick epitaxial layers the depletion at the surface of the vertical P^+N junction is not influenced by the horizontal junction and hence breakdown voltage is determined by the P^+N junction. The electric field pattern along the surface and the axis of symmetry for this case is given in fig. 1a. Going to thinner layers however, the depletion of the vertical P^+N junction becomes more and more reinforced by the horizontal junction. Consequently at the same applied voltage, the depletion stretches along the surface over a much longer distance than would be expected according to a simple one-dimensional calculation. Now the electric field at the surface is far below the critical field (Fig. 1b) and a much higher voltage can be applied before breakdown occurs. Beneath a certain thickness of the epitaxial layer, this REduced SURface Field will not reach the critical value not even at high voltages and hence

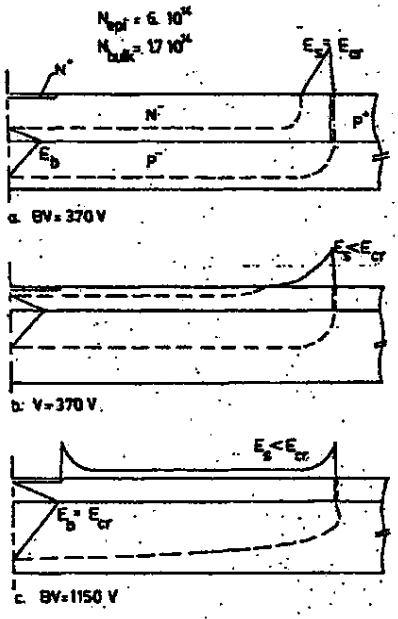

Fig. 1. Representation of the electric field distribution.
a. for a thick epitaxial layer (370 V),
b. for a thin epitaxial layer (370 V),
c. for a thin epitaxial layer (1150 V).

surface breakdown has been eliminated. Now the breakdown of the diode is determined by the horizontal junction and thus the ideal bulk breakdown can be reached. (Fig. 1c). However, since the epitaxial layer is fully depleted a new effect arises. Due to the curvature of the N^+ contact the electric field will strongly increase. For very thin epitaxial layers the effect becomes so pronounced that

the electric field peak at the edge of the N^+ region is larger than the field in the bulk.
Now corner breakdown will occur at a voltage which is lower than the ideal bulk breakdown voltage. Two-dimensional numerical calculations show that a symmetrical electric field distribution at the surface is obtained, when $N_{epi} \cdot d_{epi} = 10^{12}$ at/cm^2, where N_{epi} and d_{epi} are the doping concentration and the thickness of the epitaxial layer, respectively. For the structure as discussed so far, a plot of breakdown voltage versus epitaxial layer thickness is given.

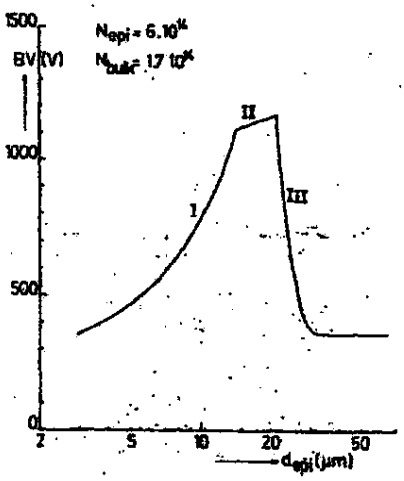

Fig. 2. Breakdown voltage as a function of epitaxial layer thickness. In region II breakdown takes place at the horizontal junction. In region I and III breakdown takes place at the N^+ or P^+ regions, respectively.

LATERAL BIPOLAR TRANSISTOR

A minor change in the diode structure leads to a high voltage bipolar transistor. Simply by introducing an N^+ emitter diffusion in the P^+ isolation region, a transistor is obtained. (Fig. 3). To make transistor action more efficient, it is preferred to enlarge the P^+ region by a shallow P^+ base diffusion.

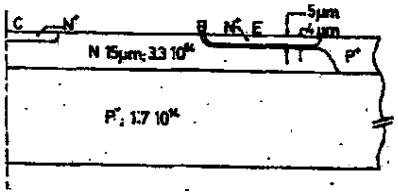

Fig. 3. Cross-section of a lateral bipolar transistor.

The high-ohmic N^- region together with the N^+ contact diffusion forms the collector zone of the transistor. The transistor action itself mainly takes place in the top-layer of the structure. By increasing the resistivity of the substrate, high emitter-collector breakdown voltages can be obtained. The P^+ base-diffusion need not necessarily be connected to the isolation region but can also be made as a floating island in the N^- layer.
Fig. 4 presents the current-voltage characteristics of an NPN lateral transistor made in an epitaxial layer with a thickness of 15 /um.

Fig. 4. Common emitter output characteristics of a lateral bipolar transistor. BV_{CEO} = 730 V BV_{CBO} = 850 V.

VERTICAL BIPOLAR TRANSISTOR

Fig. 5 shows a cross-section of a vertical PNP transistor. The only difference with a conventional structure is an additional N^- layer which is laterally bounded by a P^+ diffusion.

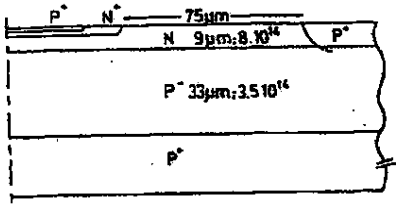

Fig. 5. Cross-section of a vertical bipolar PNP transistor.

In contrast with the lateral transistor, the Resurf N⁻ layer, is now a part of the base region. By a proper choice of dimensions and doping concentration of the N⁻ layer, the electric field distribution at the surface can be such that breakdown will take place at the horizontal N⁻P⁻ junction. In this way even with shallow base diffusions very high collector-base breakdown voltages can be obtained.
Fig. 6 shows the measured I-V characteristics of such a PNP transistor.

Fig. 6. Vertical PNP Resurf transistor made according to the principle described. BV_{CBO} = 470 V; BV_{CBO} = 520 V.

JUNCTION FET

In conventionally fabricated J-Fets a high gate-to-drain breakdown voltage is inherently coupled with a thick high-ohmic layer in order to be able to accommodate the applied reverse voltage at the drain end.
The use of Resurf layers opens the possibility of making high-voltage J-Fets with a low pinch-off voltage and a high current-carrying capability, in relatively thin epitaxial or implanted layers.

Fig. 7 shows a cross-section of a thin layer Resurf J-Fet.

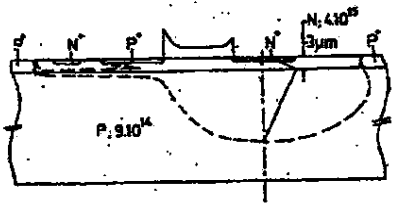

Fig. 7. Cross-section of a Resurf J-Fet.

The extension of the depletion layer in the substrate as well as the electric field distribution in the bulk and at the surface of the drain end are depicted. I-V characteristics of some experimental samples made with non-optimized photo masks are shown in Figs. 8 and 9.

Fig. 8. Resurf J-Fet made in 3 µm thick epitaxial layer. BV_{S-D} ≥ 230 V.

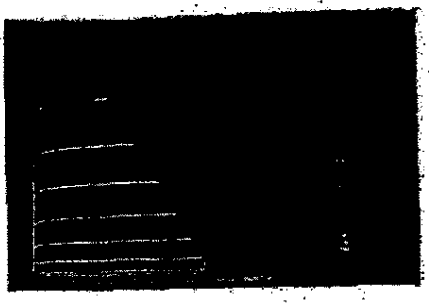

Fig. 9. Resurf J-Fet made in a 15 µm thick epitaxial layer.

CONCLUSION

The use of high-ohmic substrates with relatively thin epitaxial layers on them, which meet the requirements mentioned in this paper (i.e. $N_{epi} \times d_{epi} \geq 10^{12}$ at/cm^2) opens the possibility of making high-voltage devices whose structure and operation, in particular the electric field distribution, differ essentially from those of conventional devices.

Ref.
1) Late News Paper, ESSDERC '79 München.

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PHILIPS JOURNAL OF RESEARCH — Vol. 35 No. 1 — pp. 1-94 — 1980

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Date of publication: March 13, 1980

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Philips J. Res. 35, 1-13, 1980 *R 1008*

THIN LAYER HIGH-VOLTAGE DEVICES
(RESURF DEVICES)

by J. A. APPELS, M. G. COLLET, P. A. H. HART, H. M. J. VAES and J. F. C. M. VERHOEVEN

Abstract

The application of thin epitaxial or implanted layers in high-voltage devices is described. By means of these layers the applied reverse voltage is laterally equally distributed along the surface. In this way it is possible to make high-voltage devices even with relatively thin layers. Because of the fact that, compared with conventional devices, crucial changes in the electric field distribution take place at or at least near the surface, the acronym RESURF was chosen, which stands for REduced SURface Field.

1. Introduction

In general, high-voltage devices are associated with high-ohmic silicon, thick layers and deep diffusions. For instance in a conventional bipolar integrated circuit, the C–B voltage is built up between the p^+ base region and the n^+ buried layer. Assuming that the base and buried layer junction curvatures are sufficiently large, the breakdown voltage BV_{CBO} is mainly determined by the resistivity and thickness of the n^- layer between base and buried layer. The resistivity of the p^- substrate must of course be sufficiently high to withstand the desired voltage. Aiming at higher voltages means the use of higher ohmic substrates and epitaxial layer material, a greater distance between base and buried layer and deeper diffusions or special precautions to avoid junction curvature breakdown. The deep isolation diffusions, e.g. about 40 μm for a 200 V (BV_{CBO}) process, present particularly difficult problems.

It will be shown that it is possible to make high voltage transistors (BV_{CBO} > 1000 V) with a technique which, in contrast with conventional techniques, allows the use of relatively thin epitaxial layers (3–15 μm). The description of the mechanism is given with the aid of a diode structure.

2. Description of the mechanism

The phenomenon of high breakdown voltages in structures with thin epitaxial layers was first studied in a somewhat deviating diode structure as shown in fig. 1. Two of these diodes, which were identical except for the thickness of the epitaxial layer, were investigated. It was found that the diode with the thinner layer μm) exhibited a considerably higher breakdown voltage than the

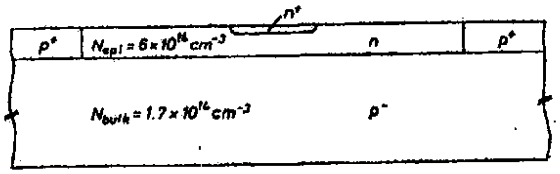

Fig. 1. Cross-section of a thin epitaxial layer diode structure. The RESURF diode.

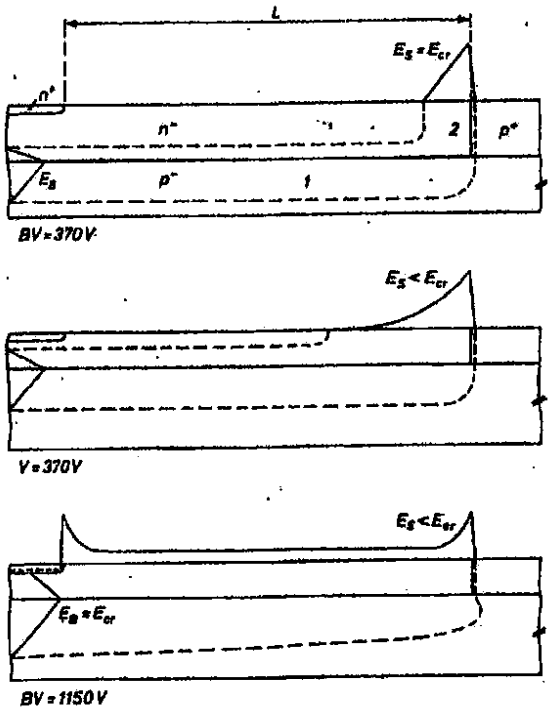

Fig. 2. Representation of the electric field distribution. $N_{epi} = 6 \times 10^{14}$ cm^{-3}; $N_B = 1.7 \times 10^{14}$ c (a) for a thick epitaxial layer (50 μm), $BV = 370$ V; (b) for a thin epitaxial layer (15 μm = 370 V; (c) for a thin epitaxial layer (15 μm), $BV = 1150$ V.

one with a thicker layer (50 μm), i.e. 1150 V and 370 V, respectively. In order to understand this, let us consider the structure shown in fig. 2, being a diode with a very thick epitaxial layer. The distance L (n^+ to p^+) is assumed to be many times larger than the epitaxial thickness. Both at the horizontal junction (1 in fig. 2*a*) below the n^+ region and at the surface of the vertical junction (2 in fig. 2*a*) the depletion behaviour can be approximated by the plane junction model. In this case the depletion at the vertical junction is one-sided, in contrast with the horizontal junction, where the depletion is two-sided. Therefore the critical field will first be reached at the surface.

Therefore, if the surface field could be reduced, it would be possible to apply a much higher voltage until the critical field at the horizontal junction was reached.

This now is exactly what happens when the epitaxial layer is made thinner. The influence of the depletion from the bottom-side at the vertical junction then becomes considerable. This is illustrated in fig. 2*b*. It can be seen that, due to the interaction of the vertical and horizontal junction parts the depletion layer stretches along the surface over a much longer distance than in the plane junction case (fig. 2*a*), which means a strong reduction of the electric surface field E_s. Further increase of the reverse voltage will finally lead to total depletion of the layer (fig. 2*c*). In a way the vertical junction can now be considered to be disconnected from the n^+ contact by depletion from the bottom-side. The structure may also be compared with a J-Fet, the n^- epitaxial layer being the channel to be pinched off and the p^- substrate acting as the gate electrode. The electric field at the vertical junction then will increase only moderately with higher voltages applied.

If one states that complete depletion of the epi-layer has to have taken place before the electric field at the vertical junction can exceed a critical field-strength, then the epitaxial layer width and the dope concentration have to fulfil the following condition.

$$N_{epi} \times d_{epi} < \frac{\varepsilon_0 \varepsilon_{si} E_{cr}}{q(1 + N_{epi}/N_B)^{\frac{1}{2}}}, \qquad (1)$$

where N_{epi} and N_B are respectively the doping concentration of the epitaxial layer and of the substrate (atoms/cm^3);
d_{epi} is the thickness of the epitaxial layer (cm);
ε_0 is the permittivity of free space (F/cm);
ε_{si} is the dielectric constant of silicon;
E_{cr} is the critical field strength (V/cm);
q is the electron charge (C).

This relation follows directly from the one-dimensional Poisson equation upon application of the classical depletion approximations. For the diode as depicted in fig. 2, this formula results in

$$N_{epi} \times d_{epi} < 6.9 \times 10^{11}\ \mathrm{cm}^{-2}.$$

Two-dimensional numerical calculations show that the optimum breakdown will be obtained when

$$N_{epi} \times d_{epi} \cong 10^{12}\ \mathrm{cm}^{-2}.$$

This indicates that purely one-dimensional analysis strictly speaking cannot be applied, but can only be used for first-order estimates.

Theoretically, for the horizontal part of the junction the breakdown voltage is given by

$$BV = \frac{\varepsilon_0\, \varepsilon_{si}\, E_{cr}^2}{2qN_B} + E_{cr}\, d_1 - \frac{qN_{epi}\, d_1^2}{2\varepsilon_0\, \varepsilon_{si}}, \qquad (2)$$

where: d is the thickness of the epitaxial layer between the n^+ contact and the p^- substrate.

In figure 2c the electric field for this situation has been depicted. As the total voltage is represented by the integral of the electric field, it can easily be seen that just by increasing the resistivity of the p^- substrate one increases the breakdown voltage.

When the voltage is increased after total depletion of the n^- layer, depletion will go on further in the n^+ contact diffusion and at the other side mainly in the p^- bulk material. At the curvature of the n^+ region one then finds local enhancement of the electric field. This may lead to earlier breakdown than would be expected from (2).

In order to elucidate the above and to see how the distance L, the dope concentrations and the thickness of the epitaxial layer have to be optimized to achieve maximum breakdown voltage, we have depicted some field configurations in fig. 3. The diode structure is symmetrical with respect to the x axis. When a voltage is applied in the reverse direction between the n^- region (via the n^+ contact region) and the p^- region, a variation of the field strength distribution E_s occurs along the surface according to the line S, while in the vertical direction the field strength E_B varies according to the line B. In practice the n^+ region will often be a diffused region; in such a region maximum curvature occurs slightly below the surface. For clarity, however, the maximum field s ;th is assumed here to be at the surface.

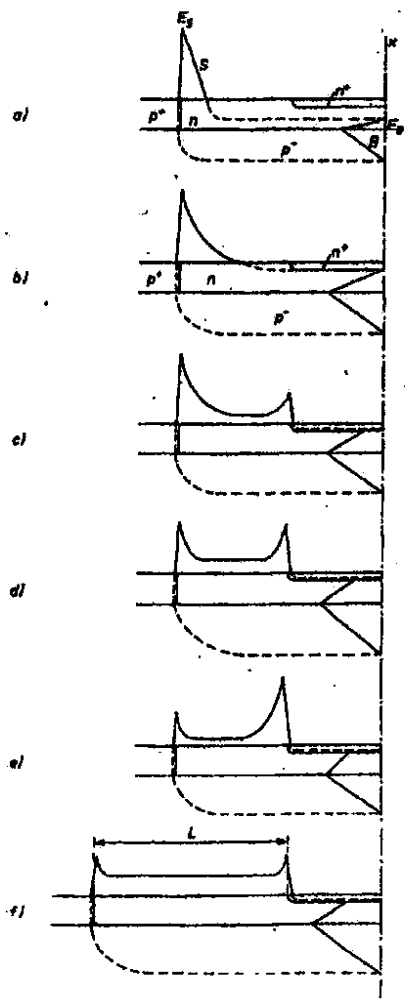

Fig ome possibilities of electric field distribution at the surface and in the bulk.

Figure 3*a* shows the case in which full depletion of the n^- layer does not occur at the breakdown voltage. The depletion at the surface of the vertical junction is still one-dimensional, the field strength at this junction is much higher than at the horizontal junction and breakdown will occur at the surface.

Figure 3*b* shows the case where the depletion at the vertical junction is already considerably influenced by the bottom junction. The depletion at the surface now extends over a greater distance. This already means a higher breakdown voltage, but still breakdown occurs at the surface. This change can be brought about by a reduction of epi-layer thickness or dope concentration.

Figures 3*c* to 3*d* show cases in which the doping concentration N and the thickness d of the epitaxial layer are such that, prior to the occurrence of surface breakdown at the vertical p^+–n^- junction, the layer is fully depleted from the horizontal junction up to the surface. Over a part of the track between the p^+ and n^+ regions the field strength E_s along the surface is constant, whereas peaks are formed in the fieldstrength distribution both at the p^+–n^- and the n^+–n^- junction. The case of fig. 3*c* may be obtained from that of fig. 3*a*, by reducing the thickness of the epitaxial layer at a fixed doping or by reducing the doping at constant epilayer thickness.

Figure 3*d* depicts the more favourable case, where the doping concentration and the thickness of the epitaxial layer are such that the two field strength peaks at the surface are substantially equal. Even in this case breakdown at the surface may still occur when the maximum field strength E_s at the horizontal junction is smaller than the maxima at the surface.

Figure 3*e* shows the reverse case of fig. 3*c* as regards surface field strength. In this case the field strength at the n^+ region is much higher than that at the p^+–n^- junction. Such a case may occur, for instance, when the epitaxial layer has a very high resistivity and the layer is already depleted long before the breakdown voltage at the vertical junction is reached. Breakdown may then occur at the edge of the n^+ region.

Figure 3*f* finally shows a case where the maximum field strength at the surface at an arbitrary reverse voltage is lower than the maximum field strength at the horizontal junction. This can be realized by a judicious choice of doping and thickness of the n^- layer and by increasing the distance L with a given doping concentration of the p substrate.

Breakdown in this case will always occur within the semiconductor body at the horizontal p–n junction. An impression of how the breakdown voltage depends on the doping concentration of the epitaxial layer is given in fig. 4. For a given p substrate ($N_A = 1.7 \times 10^{14}$/cm^3) and an epitaxial layer thickness (d_{epi}) of 15 μm, N_D is varied. ($L \gg d_{epi}$). As mentioned already, the optimum break[illegible]n voltage is found at that point of the curve where $N_{epi}\, d_{epi} \cong 10^{12}$

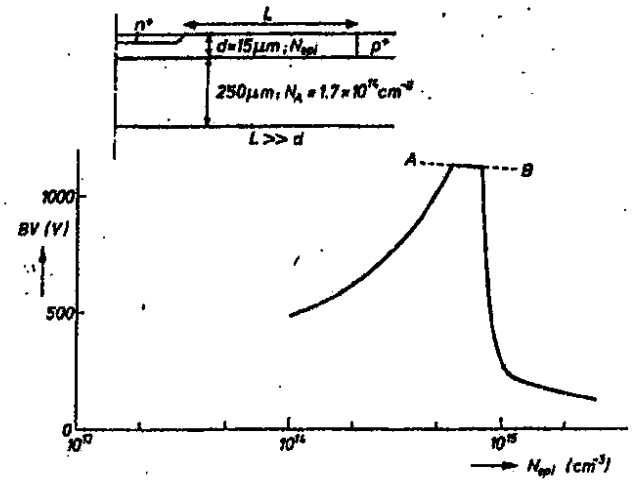

Fig. 4. Breakdown voltage as a function of the doping concentration of the epitaxial layer. L, d_{epi} and substrate doping concentration are kept constant.

The dotted line *A–B* represents the theoretical breakdown voltage of the flat n^+–n^-–p^- horizontal junction as a function of the doping concentration of the epitaxial layer (see formula (2)).

3. Some applications and results

3.1 *Lateral devices*

3.1.1. Bipolar RESURF transistor

Starting with the diode as described above, a minor change in the structure leads to a high voltage transistor. A transistor is obtained, simply by introducing an n^+ diffusion in the p^+ isolation region. To make transistor action more efficient, it is preferred to enlarge the p^+ region by a shallow p^+ base diffusion (see fig. 5.) The high-ohmic n region together with the n^+ contact diffusion forms the collector zone of the transistor. The resulting transistor has a very hi[illegible]llector–base breakdown voltage (850 V) and due to its specific structure

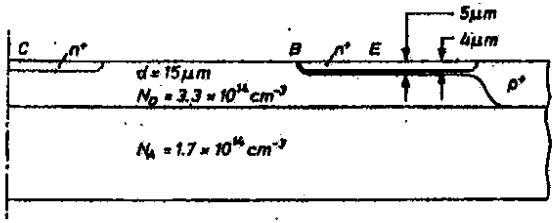

Fig. 5. Cross-section of a lateral bipolar transistor structure. For clarity only half of the transistor has been drawn.

Fig. 6. Common-emitter output characteristics of a lateral bipolar transistor. BV_{CEO} = 850 V; BV_{CBO} = 730 V.

a BV_{CEO}, which is much higher than would be expected for conventional bipolar transistors*).

Figure 6 shows the measured common-emitter output characteristics of a transistor made according to the principle described. The most important technological data are given in the structure depicted in fig. 5. As can be seen in this figure the base region is connected to the p substrate, which means that in the case of integrated circuits all base regions are interconnected. If wanted, the base region can also be made as a floating island in the n layer, without having contact with the p substrate, thus making integration possible.

3.1.2. RESURF junction fet

In conventionally fabricated J-Fet's (see fig. 7*a*) a high gate-to-drain breakdown voltage is inherently coupled with a thick high-ohmic N layer in order to be able to accommodate the applied reverse voltage at the drain end. For a given channel thickness a and layer doping concentration N, the pinch-off voltage is given by

$$V_P = -\frac{a^2\, qN_D}{8\varepsilon_{si}\,\varepsilon_0} + \Phi_M \qquad (3)$$

and the channel conductance by

$$G_0 = \frac{Wq\mu N_D a}{l}, \qquad (4)$$

where: a is the channel depth at zero bias;
q is the electron charge;

*) J. A. Appels, M. G. Collet, P. A. H. Hart, H. M. J. Vaes and J. F. C. M. Verhoeven, Thin ... er high-voltage devices (RESURF devices), Late news paper, presented at ESS ..., 1979, München.

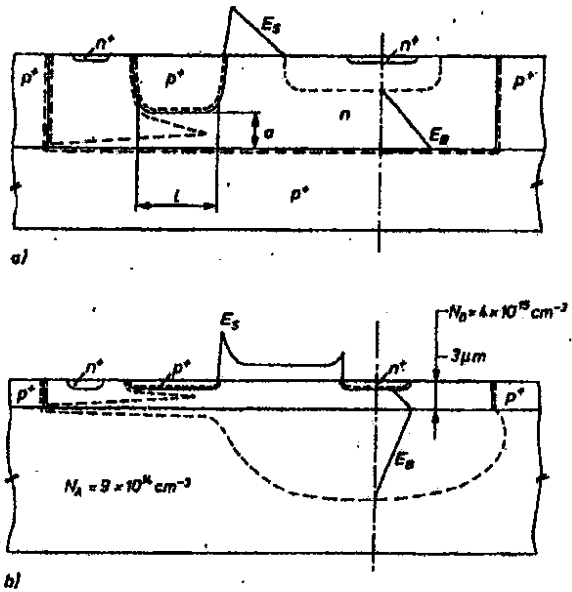

Fig. 7 (*a*) Cross-section of a conventional J-Fet. The channel depth has been denoted by a and channel length by l. (*b*) Cross-section of a RESURF J-Fet. For clarity only the electric field distribution at the most important places has been drawn.

N_D is the channel doping concentration;
ε_{si} is the dielectric constant of silicon;
ε_0 is the permittivity of free space;
Φ_{bi} is the built-in voltage;
W is the channel width;
l is the channel length;
μ is the drift mobility in the channel.

In order to achieve higher breakdown voltages, N_D must be decreased, e.g. with a factor β to $N_D' = N_D/\beta$ ($\beta > 1$). To keep V_p constant, according to eq. (3), a must then be increased up to $a' = a\sqrt{\beta}$. Upon substitution into eq. (4) it is found that this will lead to a reduced channel conductance G_0'

$$G_0' = G_0/\sqrt{\beta}. \tag{5}$$

The use of thin epitaxial or implanted layers that meet the requirements described above, opens the possibility of making high-voltage J-Fets with a low pinch-off voltage and yet a high current-carrying capability.

A comparison between a conventional and a thin layer structure will make this clear.

	conventional	RESURF performance
N_D	8×10^{14} cm^{-3}	3.3×10^{15} cm^{-3}
$N_{substr.}$	5×10^{15} cm^{-3}	5×10^{14} cm^{-3}
a	6.2 μm	2 μm
V_p	5.35 V	4.9 V
G_0	1.03×10^{-4} Ω^{-1}	1.34×10^{-4} Ω^{-1} (for $W/l = 1$)
BV	230 V	300 V
d_{epi}	15 μm	3 μm
I_{DSS}	1.48×10^{-4} A	1.74×10^{-4} A (for $W/l = 1$)

The most striking differences are that the substrate dope has been reduced drastically to make it possible to store the applied voltage in the bulk, and the epitaxial layer thickness has decreased from 15 μm to 3 μm[1]).

Because of the spread in thickness and doping concentration of epitaxial layers together with deep isolation and gate diffusions, the reproducibility of conventional high voltage J-Fets will be very poor.

An additional advantage of the thin layer technique is that when going to layer thicknesses of about 3 μm, ion implantation becomes very attractive. This has not only the advantage of a better control of the doping concentration but it offers the possibility of making the n layer locally.

To point out the differences once more, the two structures are shown together in fig. 7 on a more or less comparable scale. The situation as depicted is at a voltage of about 150 V, which is much lower than the breakdown voltage. The field distribution in the bulk and at the surface is essentially different for the two structures. In contrast with the conventional structure, the epitaxial layer of the thin layer device is already fully depleted at the drain end.

Of course the application of the RESURF technique for lateral devices is not restricted to bipolar and junction field effect transistors.

3.2. *Vertical devices*

In figure 8 a vertical discrete p–n–p transistor is shown. The structure is identical with that of a conventional one, except that an additional n layer is introduced, which is laterally surrounded by a p^+ diffusion. The n layer is part of the base region and has such a doping concentration and thickness that it is already fully depleted at a relatively low voltage.

By choosing the proper dimensions and doping concentration of the n layer a high collector–base breakdown can be obtained even with a very shallow n^+ base diffusion.

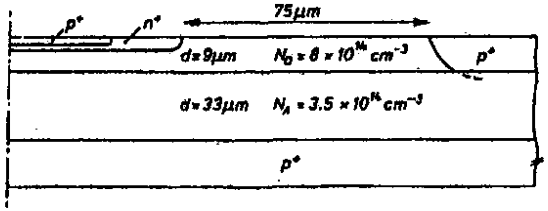

Fig. 8. Cross-section of a vertical bipolar RESURF transistor made according to the technique described.

In this example the base diffusion used is only 5.5 μm deep. If conventionally made, this transistor would exhibit, due to base junction curvature, a base–collector breakdown of about 250 V. Introduction of the n^- epitaxial layer has improved the breakdown voltage to 550 V, which is about the theoretical value for flat collector–base breakdown in this structure.

The common-emitter output characteristics of this transistor are shown in fig. 9. Under certain conditions the n layer unfavourably affects the transistor performance. Though at some cost of the breakdown voltage, the n^+ base r penetration can in such conditions be chosen deeper with respect to

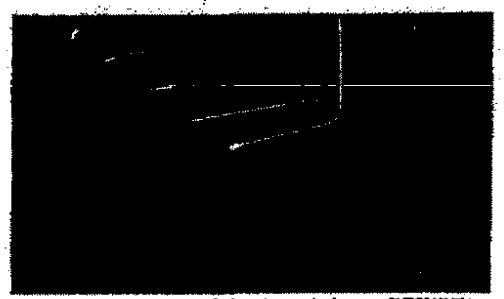

Fig. 9. Common-emitter output characteristics of a vertical p–n–p RESURF transistor. BV_{CEO} = 470 V; BV_{CBO} = 520 V.

the n^- layer width. This loss of breakdown voltage can be further reduced by the usual techniques of reducing the junction curvature, e.g. by implantation through a tapered oxide. A wide n^- layer remaining underneath the base, when fully depleted, causes an increase in collector transit time. When not fully depleted it causes an increase of collector feedback capacitance.

However, when high-injection conditions prevail, it causes an increase of the base width and a deterioration of high-frequency performance. As high-voltage devices are usually rather slow devices and the shallow diffusions themselves tend to increase the speed, these disadvantages will often be offset by the ease with which the high-voltage requirements can be met.

The increase of collector capacitance will be quite small, if any, for large-area power devices. The technique described is of course not restricted to discrete vertical bipolar transistors; but can also be used e.g. for thyristors and V-groove MOST devices, as well as in integrated circuit structures.

4. Conclusion

The use of high-ohmic substrates with relatively thin epitaxial layers on them, which meet the requirements mentioned in this paper (i.e. $N_{epi}\, d_{epi} \cong 10^{12}$ at/cm^2), opens the possibility of making high-voltage devices whose structure, operation and in particular the electric field distribution, differ essentially from those of conventionally made devices.

With very shallow diffusions, especially in lateral devices, unexpectedly high breakdown voltages can be obtained. When the epitaxial layer meets the above-mentioned requirements and L (see fig. 3f) is sufficiently large, then, because of an improved distribution of the electric field at the surface of the device and at the curvatures of the junctions, maximum breakdown of the horizontal bulk ion can be obtained.

Acknowledgements

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Philips Research Laboratories *Eindhoven, October 1979*

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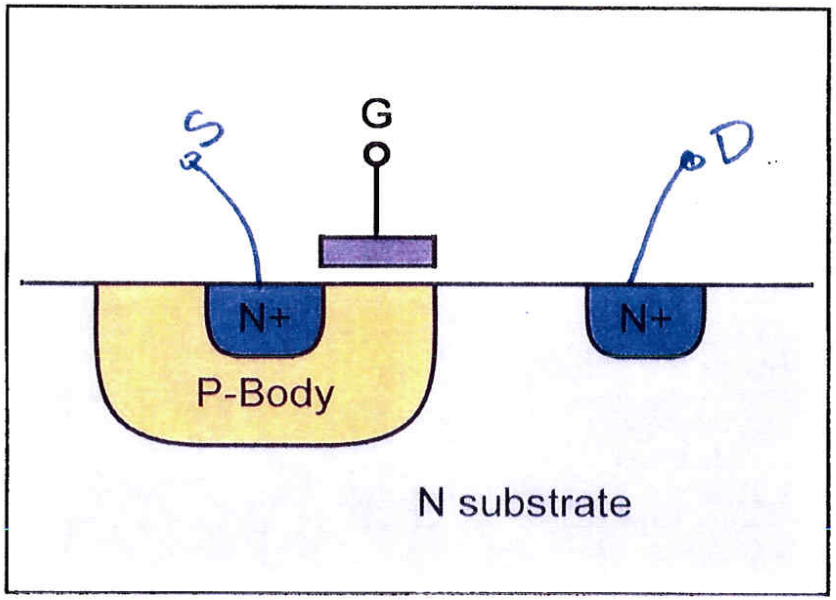

Figure A
DMOS in 1984-85

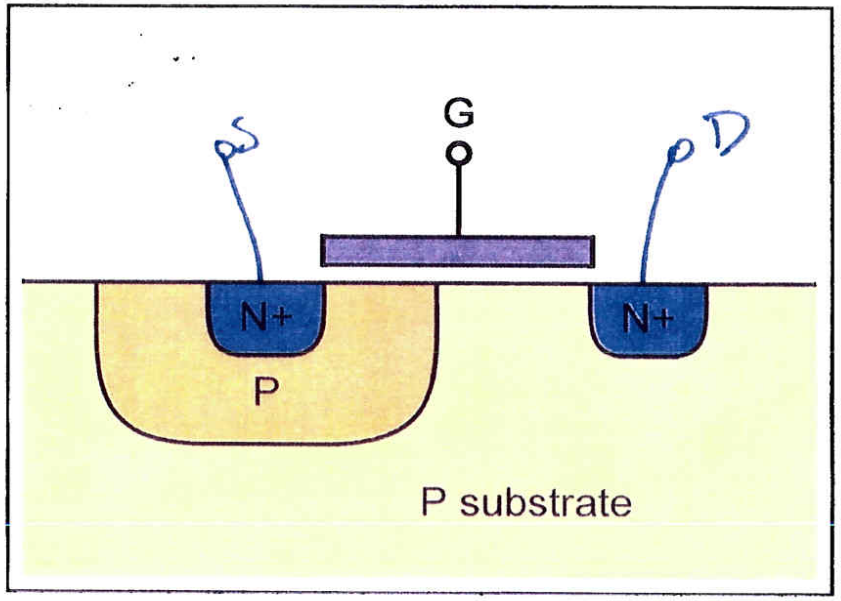

Figure B

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